Towards printed chaotic circuits: a topology based on memristors

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Abstract—**In this work a chaotic circuit for printed electronics applications has been designed. The circuit is based on the use of memristors, which provide nonlinear elements with memory and have been already implemented in flexible electronics. The design takes into account a physical model of the memristor suitable for already fabricated TiO_2 devices, in order to reduce the gap between ideal memristor-based chaotic oscillators and possible printed electronics implementations.**

Keywords-Chaotic circuits; memristor; printed electronics

I. INTRODUCTION

Since its discovery, chaos has fascinated many scientists and researchers both in the theoretical fields and in application-oriented studies. Chaos appears as a model of many natural phenomena and found applications in several devices [1]. Recently, a new chaos-based technique has been conceived for application in traceability of products [2]. Traceability is defined as the ability to trace and follow a good (in particular foods) through all the stages of production and distribution, and is today a fundamental instrument to optimize the supply chain, to guarantee the product safety and to gain competitiveness in the market [3], [4].

In particular, the idea introduced in [2] is to integrate the techniques based on traditional tools for product identification during traceability with organic circuits showing chaotic dynamics when activated by an external generator. Such circuits have intrinsic safe identificability properties, since only a copy of this circuit is able to identify it. Therefore, the information encoded in this chaotic tag can be decoded only in the presence of a circuit which can be synchronized to it. In this way, a chaotic key to make safe the identification procedure can be added to a tag also containing the information traditionally embedded in the tag.

The application therefore envisages the integration of the chaotic circuit with current low-cost technologies used in product identification such as bar codes or RFID tags. The aim of this work is to study components and topologies suitable for the implementation of a chaotic circuit in printed electronic technologies.

The key element we identified as the source of nonlinearity in the circuit is the memristor. The memristor, known as the fourth basic circuit element, was introduced to represent the relationship between flux and charge as the other basic elements represent relationships between other fundamental electrical quantities [5]. The memristor fundamental characteristics is described in terms of v=M(q) i, where M(q) is defined as the memristance and is function of the quantity of charge that has passed through the device. In a memristor, this relation is nonlinear and the v–i characteristic is a curve that takes a form of a hysteresis loop pinched in the origin. The memristor is thus a nonlinear element with memory, and, for this reason, its use as fundamental element for the design of chaotic systems is currently intensively explored [6]. The first component with a memristor characteristic was fabricated in the HP laboratory [7], after which different materials and techniques have been used to produce devices with memristive characteristics. It is worth to note that the memristor is implemented in flexible electronics using spin-on sol gel process, and there are several examples of memristors based on organic electronics [8], [9]. In this work, we design a chaotic circuit based on the mathematical model of a HP memristor oriented towards an implementation based on printed electronics.

II. MODEL OF THE HP MEMRISTOR

The HP memristor is a passive device constituted by a layer of titanium dioxide TiO_2 and an oxygen deficient layer TiO_{2-x} sandwiched between two platinum layers acting as electrodes of the device. The resistance of the whole device depends on the width of the doped region, indicated as *w(t)*, which is controlled by the amount of current that passed through the device. In fact, the doped region and the undoped one have different resistivity values. When the width of the doped region is equal to the whole thickness, the memristor has a resistance equal to R_{ON}, while, in the opposite case, when the undoped region covers the whole thickness of the device (i.e., $w = 0$), the memristor has a resistance equal to R_{OFF} . The width of the doped region is therefore assumed as the internal variable of the device which is modelled [7] as the series of two resistors, each depending on the value of *w(t):*

$$v(t) = \left(R_{ON}\frac{w(t)}{D} + R_{OFF}\left(1 - \frac{w(t)}{D}\right)\right)\mathrm{i(t)} \qquad (1)$$

where D is the whole thickness of the structure. The variable *w(t)* is limited to values between zero and D, and evolves according to the nonlinear drift model:

$$\frac{dw(t)}{dt} = \eta\frac{\mu_v R_{ON}}{D}F\left(\frac{w(t)}{D}\right)i(t) \qquad (2)$$

where η accounts for the polarity of the memristor (if $\eta=1$ the width of the region expands when a positive current is applied; if $\eta=-1$ the region contracts in correspondence of a positive input), μ_v is the average ion mobility and $F(\frac{w(t)}{D})$ is the Biolek window function [10] used to model the effect of boundary conditions and the nonlinearity of the ionic transport:

$$F(x,i) = 1 - (x - stp(-i))^2 \qquad (3)$$

where *stp(i)* is the Heaviside step function.

The fingerprint of the memristive behavior of a device is the hysteresis pinched loop which can be recovered in the v-i plane when a sinusoidal voltage input is applied to the device terminals and the current is monitored. It is important to note that, if the frequency of the sinusoidal signal is smaller with respect to the time scale of the memristor dynamics, the internal state variable *w(t)* may saturate to its boundary values, leading to a non symmetrical characteristics. In fact, when $w=0$ the memristor resistance is equal to R_{OFF}, while for $w=D$ the memristor resistance is equal to R_{ON}. Therefore, if the HP memristor model is used, a highly nonlinear behavior can be obtained, but this is not symmetrical. On the opposite, the design of many chaotic circuits is based on symmetrical nonlinearities, but, most importantly, since the idea is to use the memristor as the fundamental nonlinearity of the circuit, it has to provide a dissipating effect in correspondence of both saturation limits for the state variable *w(t)*, which is not the case of one single memristor.

For this reason, in this work we use two HP memristors connected in antiparallel, i.e., with the two terminals shortened but with opposite polarities. In such configuration, the voltage across each memristor is equal to the voltage of the resulting two-terminal device, while the current is the sum of the current through each memristor.

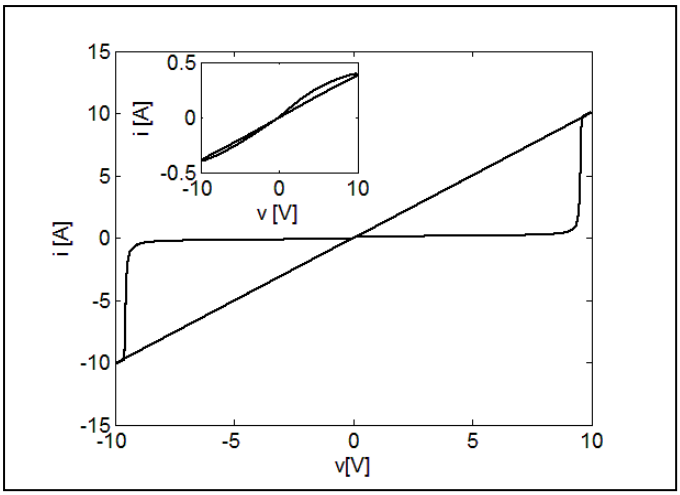

Figure 1. v-i characteristic of a configuration of two memristors connected in antiparallel. Input frequency ω=0.1 rad/s (in the inset ω=1rad/s).

Fig. 1 illustrates the behavior of this configuration. In particular, the behavior with respect to two different values of the input frequency is shown. A symmetrical behavior is obtained. The most interesting case is that corresponding to a lower input frequency. In fact, in this case the state variable *w(t)* oscillates between its boundary values. The configuration made of two HP memristors in antiparallel therefore exhibits a symmetrical, highly nonlinear behavior which has been exploited to design the chaotic circuit described in the next section.

III. THE CIRCUIT

The nonlinearity made of two HP memristors in antiparallel has been used to design a chaotic circuit. This is derived by the topology of the Chua's oscillator by replacing the Chua's diode with two HP memristors in antiparallel and a negative conductance, which is needed to implement an active element. In fact, chaos cannot be obtained in a totally passive circuit. The approach of replacing the Chua's diode, common to other chaotic circuits, relies on the universality of the topology of the Chua's circuit [11], consisting of a LC group interacting with a nonlinear dynamical subcircuit.

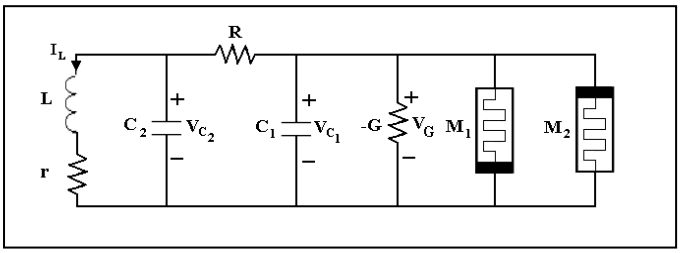

Figure 2. Scheme of the circuit.

The chaotic circuit proposed is shown in Fig. 2. It consists of two capacitors, one inductor, two resistors, a negative conductance and the two HP memristors in antiparallel. By applying the Kirchhoff voltage and current laws and the constitutive relationship of the HP memristor, the equations governing the circuit are derived as follows:

$$\begin{cases} \frac{dv_{C1}}{dt} = \frac{1}{C_1}\left(\frac{v_{C2}-v_{C1}}{R} + Gv_{C1} - \frac{v_{C1}}{R_1(w_1)} - \frac{v_{C1}}{R_2(w_2)}\right) \\ \frac{dv_{C2}}{dt} = \frac{1}{C_2}\left(\frac{v_{C1}-v_{C2}}{R} - i_L\right) \\ \frac{di_L}{dt} = \frac{1}{L}(v_{C2} - ri_L) \\ \frac{dw_1}{dt} = \frac{\eta_1 \mu_v R_{ON}}{D} F\left(\frac{w_1}{D}\right)\frac{v_{C1}}{R_1(w_1)} \\ \frac{dw_2}{dt} = \frac{\eta_2 \mu_v R_{ON}}{D} F\left(\frac{w_2}{D}\right)\frac{v_{C1}}{R_2(w_2)} \end{cases} \qquad (4)$$

where $R_i(w_i) = R_{ON}\frac{w_i}{D} + R_{OFF}\left(1 - \frac{w_i}{D}\right)$ and $\eta_1 = -\eta_2 = 1$.

We now derive a dimensionless form of Eqs. (4), by introducing the following scaled variables:

$$X = v_{C1}/v_0$$
$$Y = v_{C2}/v_0$$
$$Z = i_L/i_0$$
$$W_1 = w_1/D$$
$$W_2 = w_2/D$$
$$\tau = t/t_0$$

with:

This work has been partially supported by the APOSTILLE project.

$$v_0 = 1V, i_0 = v_0/R_{ON}\,,\ t_0 = D^2/\mu v_0\,,$$
$$C_0 = \frac{D^2}{\mu v_0 R_{ON}},\ L_0 = \frac{D^2 R_{ON}}{\mu v_0}$$

With this scaling, Eqs. (4) become:

$$\begin{cases} \frac{dX}{d\tau} = \frac{C_0}{C_1}\left(\frac{R_{ON}}{R}Y - \frac{R_{ON}}{R}X + GR_{ON}X - \frac{X}{\bar{R}_1(W_1)} - \frac{X}{\bar{R}_2(W_2)}\right) \\ \frac{dY}{d\tau} = \frac{C_0}{C_2}\left(\frac{R_{ON}}{R}X - \frac{R_{ON}}{R}Y - Z\right) \\ \frac{dZ}{d\tau} = \frac{L_0}{L}\left(X - \frac{r}{R_{ON}}Z\right) \\ \frac{dW_1}{d\tau} = \eta_1 F(W_1)\frac{X}{R_1(w_1)} \\ \frac{dW_2}{d\tau} = \eta_2 F(W_1)\frac{X}{R_2(w_2)} \end{cases} \quad (5)$$

The following typical values for the HP memristors have been used: $R_{ON} = 100\Omega, R_{OFF}/R_{ON} = 100\,, D = 10nm$ and $\mu_v = 10^{-14} cm^2 s^{-1} v^{-1}$.

Model (5) has been numerically investigated with respect to different values of the parameters. It exhibits chaos in several regions of the parameter space. An example of a chaotic attractor that can be generated by this circuit is shown in Fig. 3. This attractor is obtained for the following set of parameters: $\frac{C_1}{C_0} = 0.2564, \frac{C_2}{C_0} = 0.75, \frac{L}{L_0} = 0.2, GR_{ON} = 0.6, \frac{R}{R_{ON}} = 2.7$ and $\frac{r}{R_{ON}} = 0.01$. In correspondence of these parameters, the maximum Lyapunov exponent is equal to 0.068.

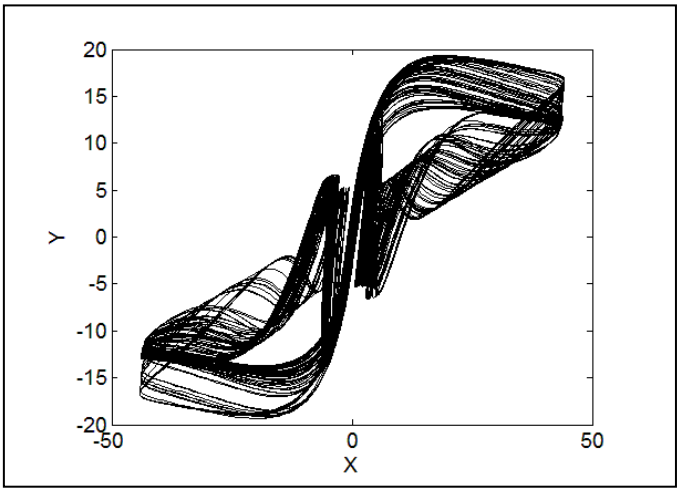

Figure 3. Chaotic attractor of the HP memristor-based oscillator: projection on the X-Z plane.

Figs. 4-7 show the bifurcation diagrams obtained with respect to the parameters of the circuit. These report the value of local maxima of the state variable *Y*. Windows of chaotic behaviors and periodic behaviors appear in the bifurcation diagrams. The analysis is confirmed by the Lyapunov spectrum (not shown).

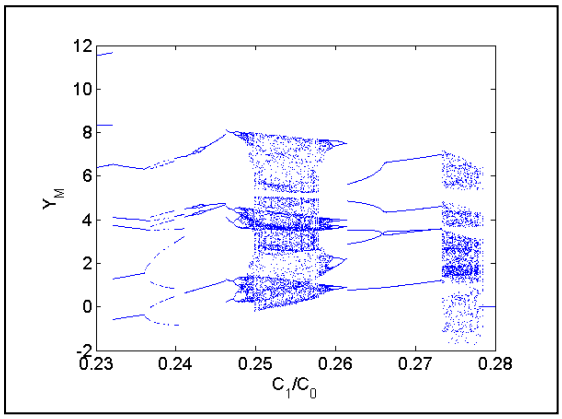

Figure 4. Bifurcation diagram with respect to C_1/C_0.

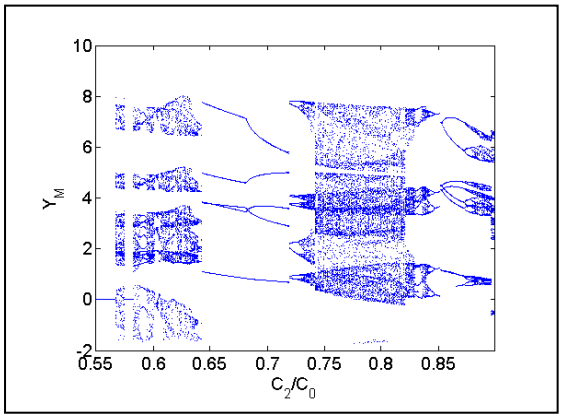

Figure 5. Bifurcation diagram with respect to C_2/C_0.

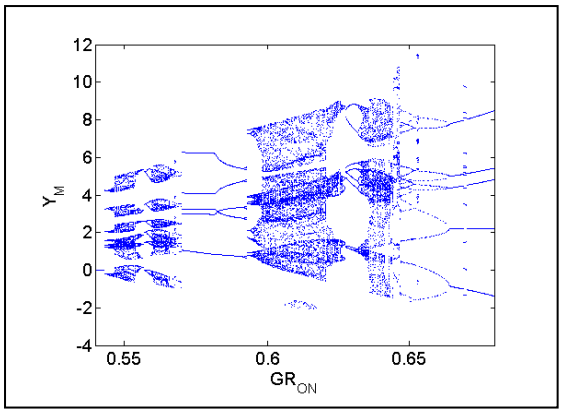

Figure 6. Bifurcation diagram with respect to GR_{ON}.

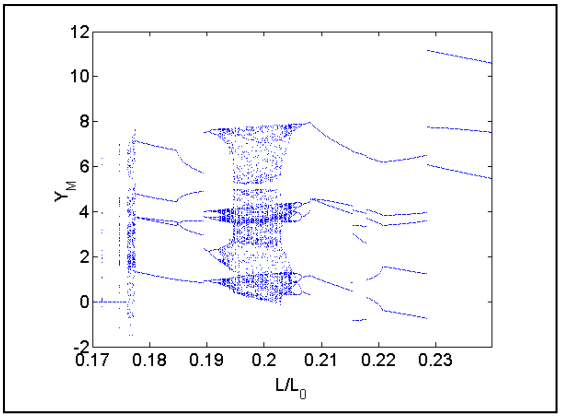

Figure 7. Bifurcation diagram with respect to L/L_0.

IV. CONCLUSIONS

In this work, we have introduced a chaotic circuit based on memristors. With respect to other memristor-based oscillators, this circuit takes into account the physical model describing the HP memristor. This model has been used to reproduce the characteristics of the TiO_2 memristor fabricated in the HP laboratories, but is quite different from other ideal curves often used in memristor-based oscillators. The circuit makes use of two HP memristors connected in an antiparallel configuration to obtain a symmetrical nonlinearity.

The HP memristor has been fabricated in flexible electronics, but other successful techniques have been applied to implement TiO_2 memristors. The idea of this work is to provide a topology which can be used to build a chaotic circuit with TiO_2 memristors, and, in particular, memristors realized in printed electronics. Printed electronics-based chaotic circuits will be low-cost and suitable for consumer market industry such as in traceability of products and goods.

The next step of the ongoing research will be oriented to the realization of a memristor in printed electronics. To do this, several issues have to be faced. First of all, the development and availability of adequate inks (and in particular TiO_2 inks) for inkjet printing are fundamental topics to be addressed [12]. Then, the choice of the materials to be used as electrodes and as substrates has to be addressed, taking also into account which processes have to performed on the TiO_2 ink to obtain a two-layer film with a barrier between regions with different oxygen vacancies concentration. These activities will be developed in the framework of the APOSTILLE project.

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