# INDEL 2018


## NBTI and Radiation Related Degradation and Lifetime Estimation in power VDMOSFETs

**D. Danković and N. Stojadinović**

*University of Niš, Faculty of Electronic Engineering*

*Serbia*

# Objective

- To develop

  a cost-effective method suitable for NBTI measurement on p-channel power VDMOSFETs

- To investigate

  -effects of static and pulsed NBT stressing on threshold voltage in p-channel power VDMOSFETs IRF9520
  -NBTI and radiation related degradation

- To analyse

  -recoverable and permanent components of $V_T$ shift in stressed devices
  -lifetime in stressed devices

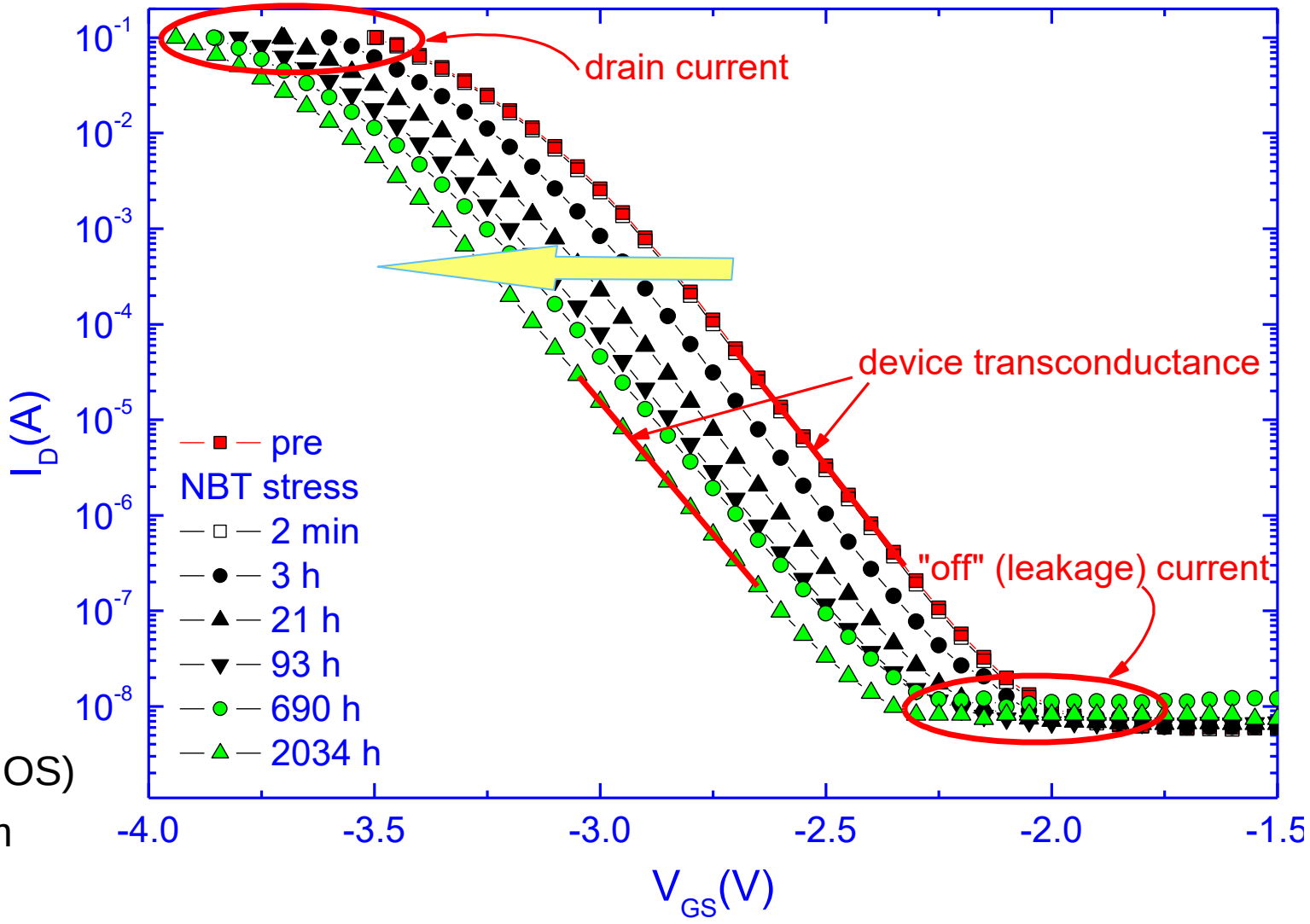
# Outline

- Introduction
- Experimental details
  - Measurement method
  - Devices
- Results and discussion
  - Static and pulsed NBT stress
  - Lifetime estimation
  - NBTI and irradiation
- Conclusions

# Introduction

- Degradation of power MOSFETs under the stresses, such as ionizing irradiation, high electric field, elevated temperature, etc., has been subject of extensive research
- **Negative Bias Temperature Instabilities (NBTI)** are critical:
  - in p-MOS devices
  - exposed to negative gate voltages (2-6 MV/cm)
  - at elevated temperatures (100-250$^{o}$C)
- The above fields and/or temperatures are typical for burn-in testing, but also can be approached during the routine operation of power MOSFETs in automotive and industrial applications

# NBTI are manifested as…



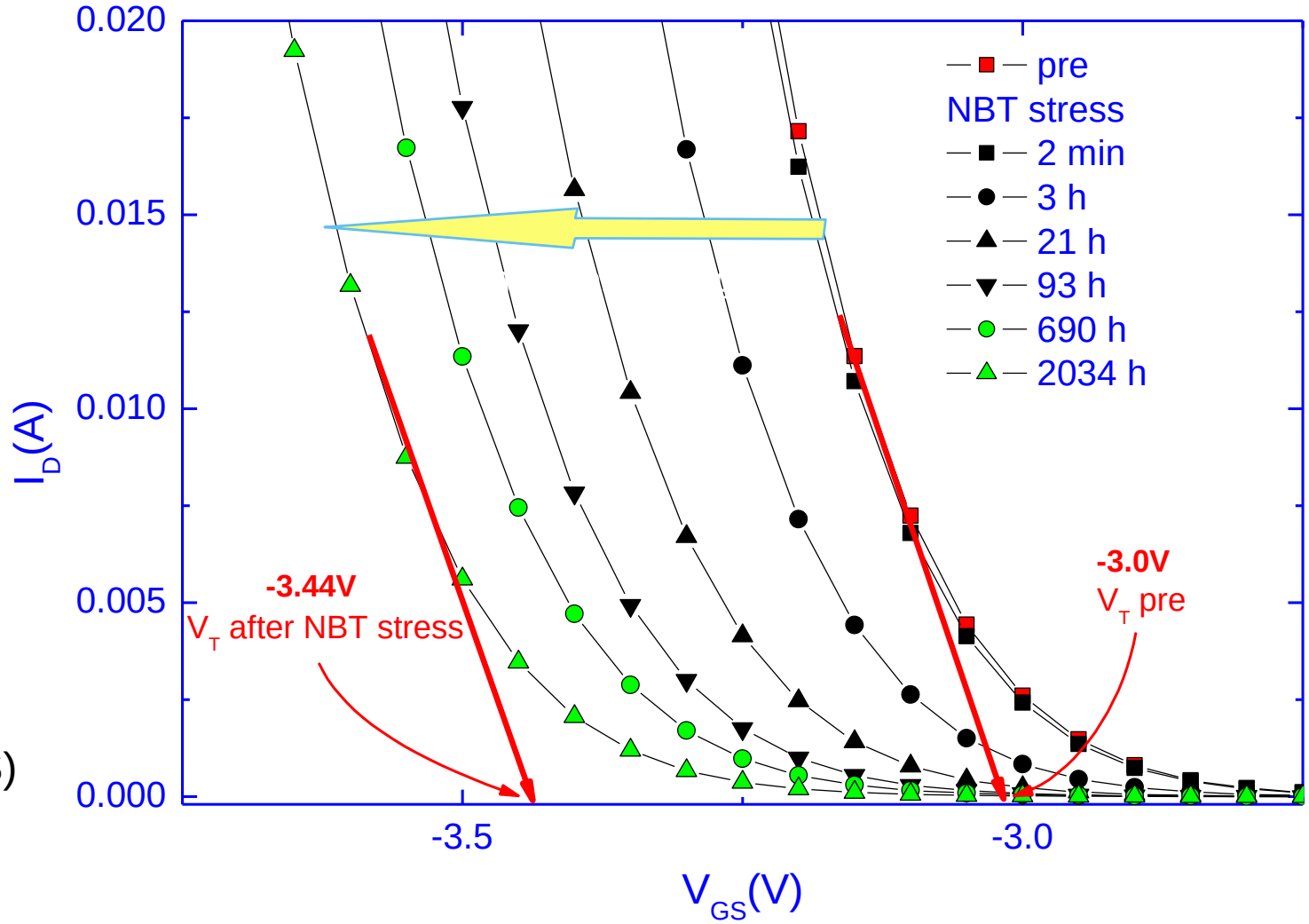

IRF9520 (pMOS)

$E_{ox}$ = 4MV/cm

$T$ = 150°C

$t_{stress}$ = 2034h

# NBTI are manifested as…




IRF9520 (pMOS)

$E_{ox}$ = 4MV/cm

$T$ = 150°C

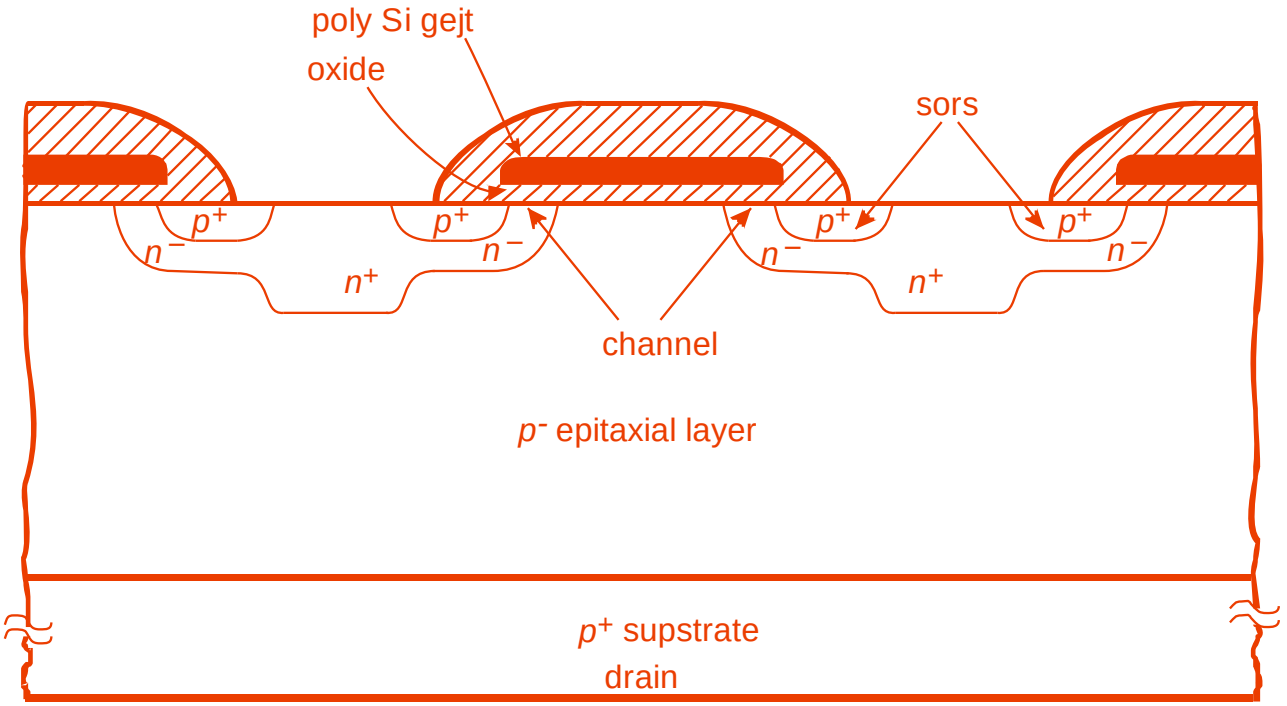
$t_{stress}$ = 2034h

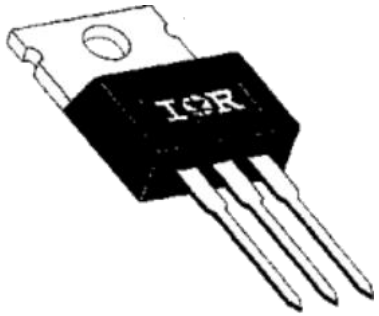
# Experimental details

- Devices:

Commercial p-channel power VDMOSFETs IRF9520 built in Si-gate technology

(6.8 A / 100 V; $V_T$ = -3.0 V; $d_{ox}$=100 nm)




**Plastic cases**

**TO-220**

# Experimental details

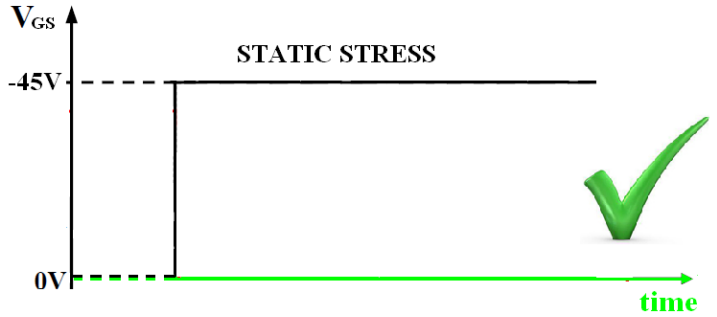
- Stress Type:

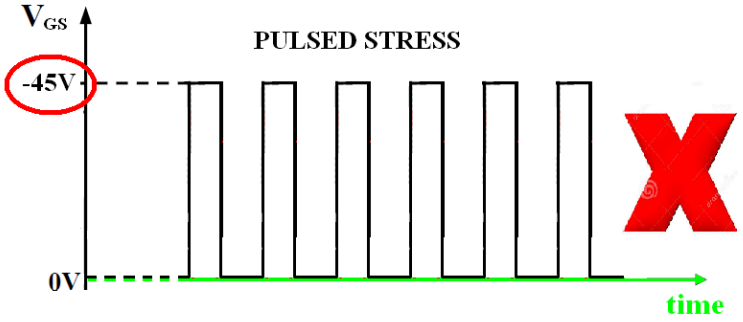
$E_{ox}$ = 2-6 MV/cm ↔ NBTI

$d_{ox}$ = 100 nm ↔ VDMOS

$V_{GS} \approx E_{ox} * d_{ox}$ → $V_{GS} \approx$ -20 ÷ -60V !!!

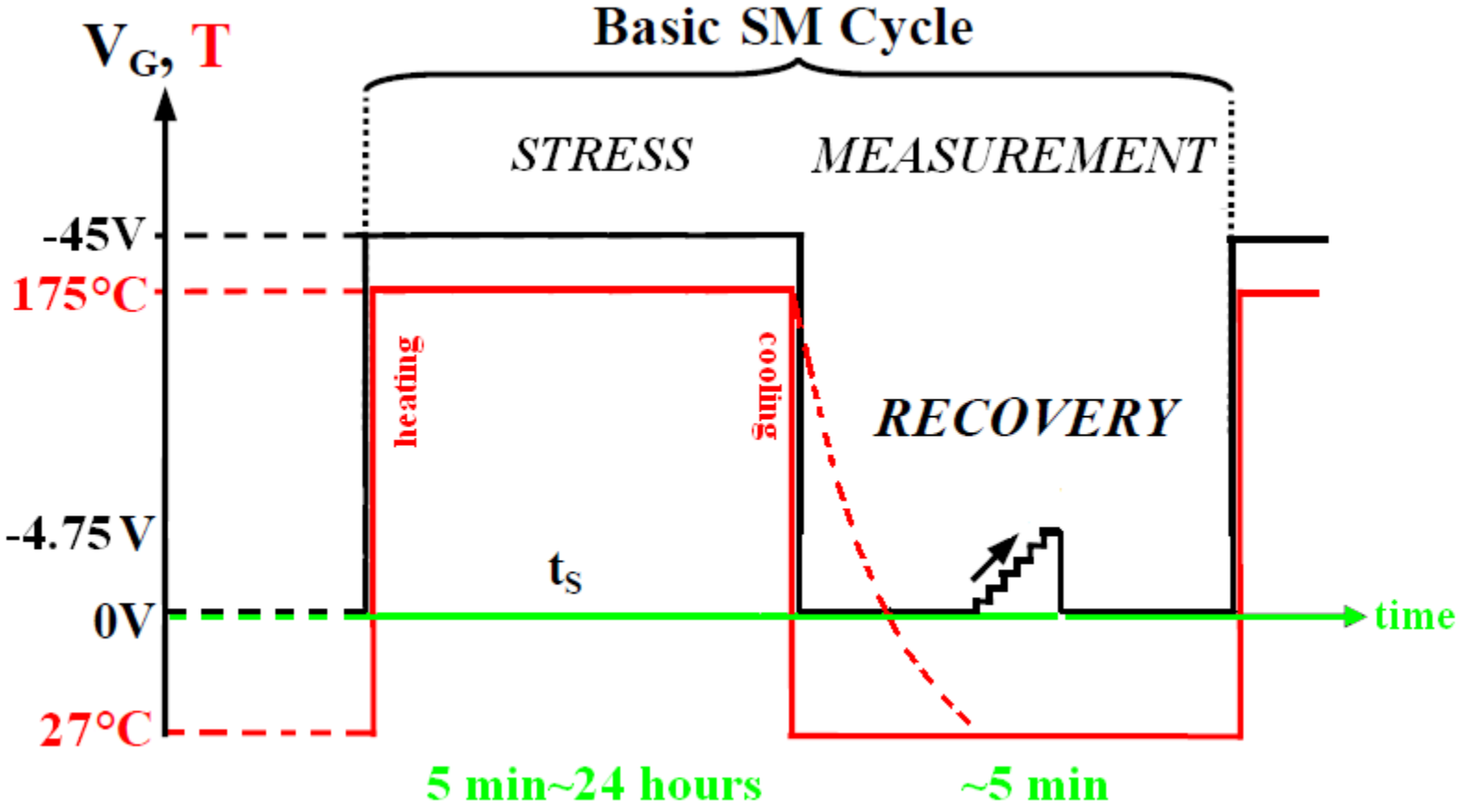
Owing to the thick gate oxide, NBT stressing of these devices required gate stress voltage amplitudes even over -20V

# Experimental details

- Measurement method: Conventional S-M-S
  (Traditional S-M-S)



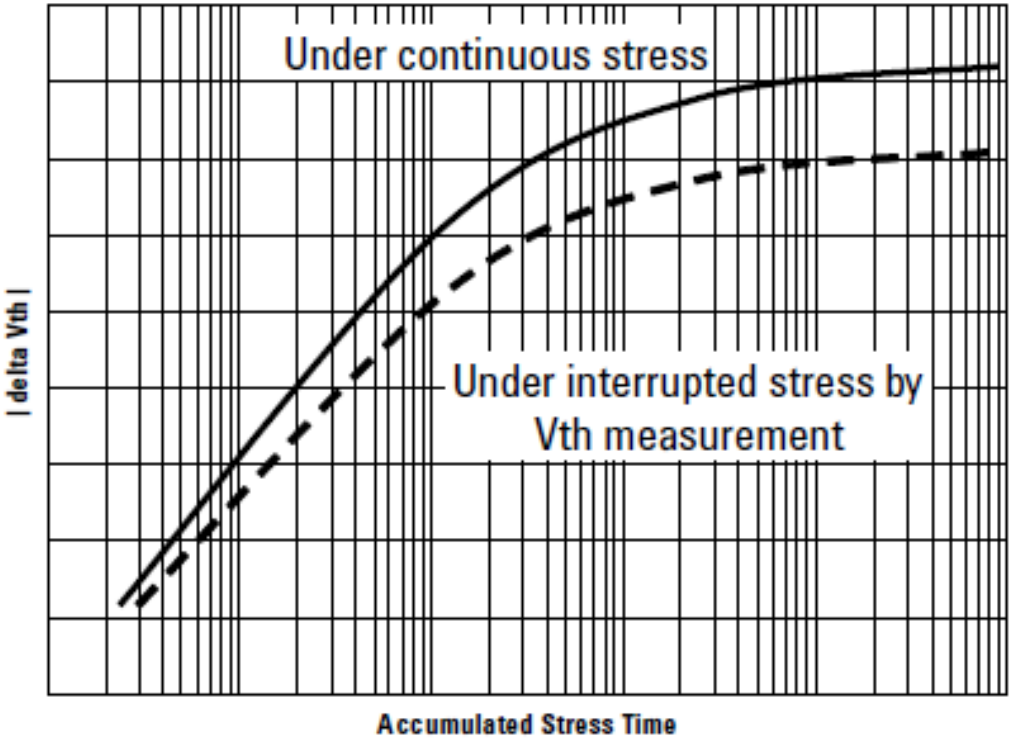
# Experimental details

- Measurement method: Conventional S-M-S

**Agilent B1500A Semiconductor Device Analyzer**

There are two problems with this traditional NBTI characterization approach:

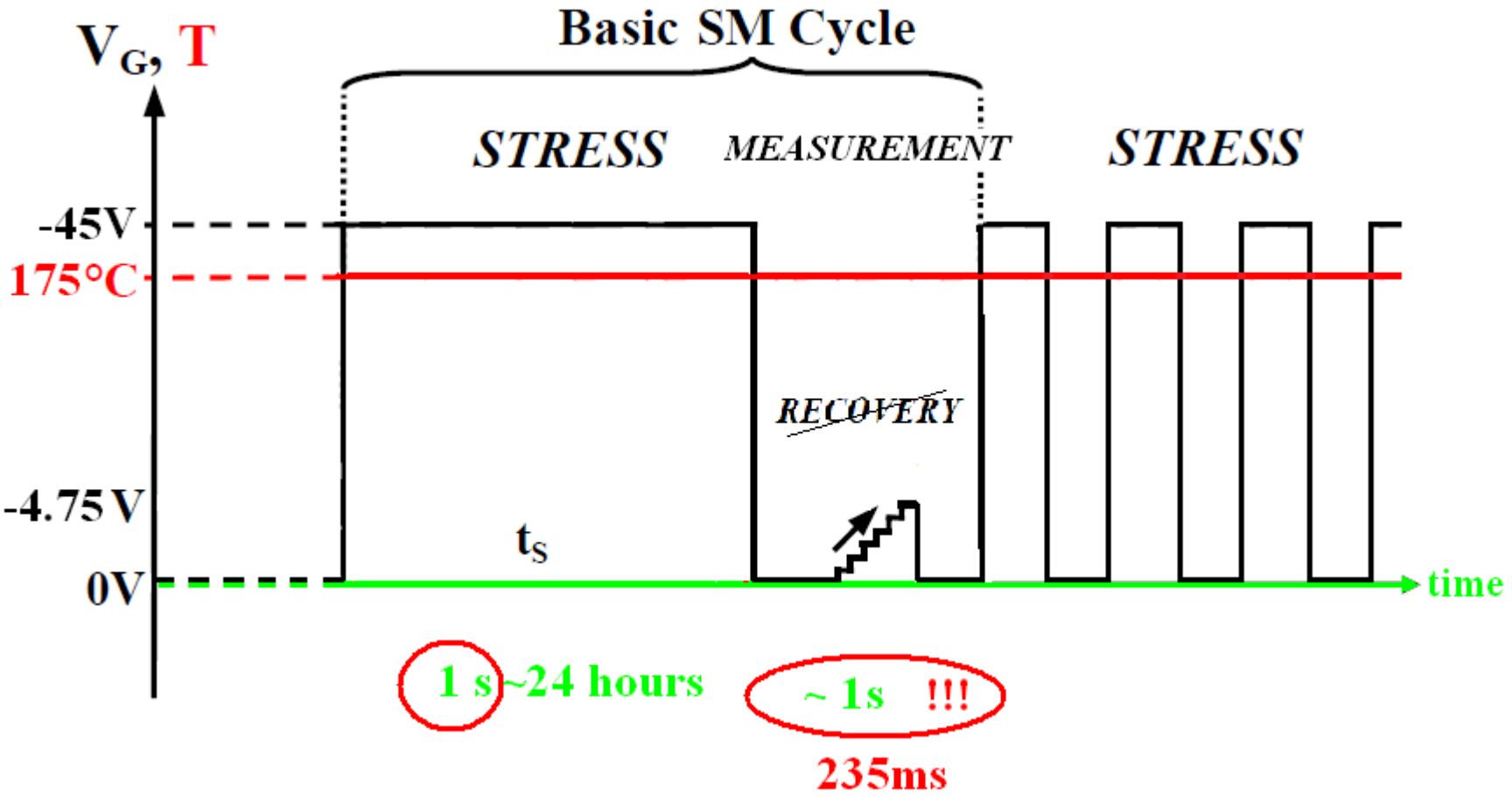
1. The stress voltage discontinuity, that occurs when the applied stress returns to zero before and after the degradation characterization, allows the device to recover from the applied stress.
2. The slow Vth measurement time also allows for recovery during the measurement phase.




Problem with traditional NBTI test

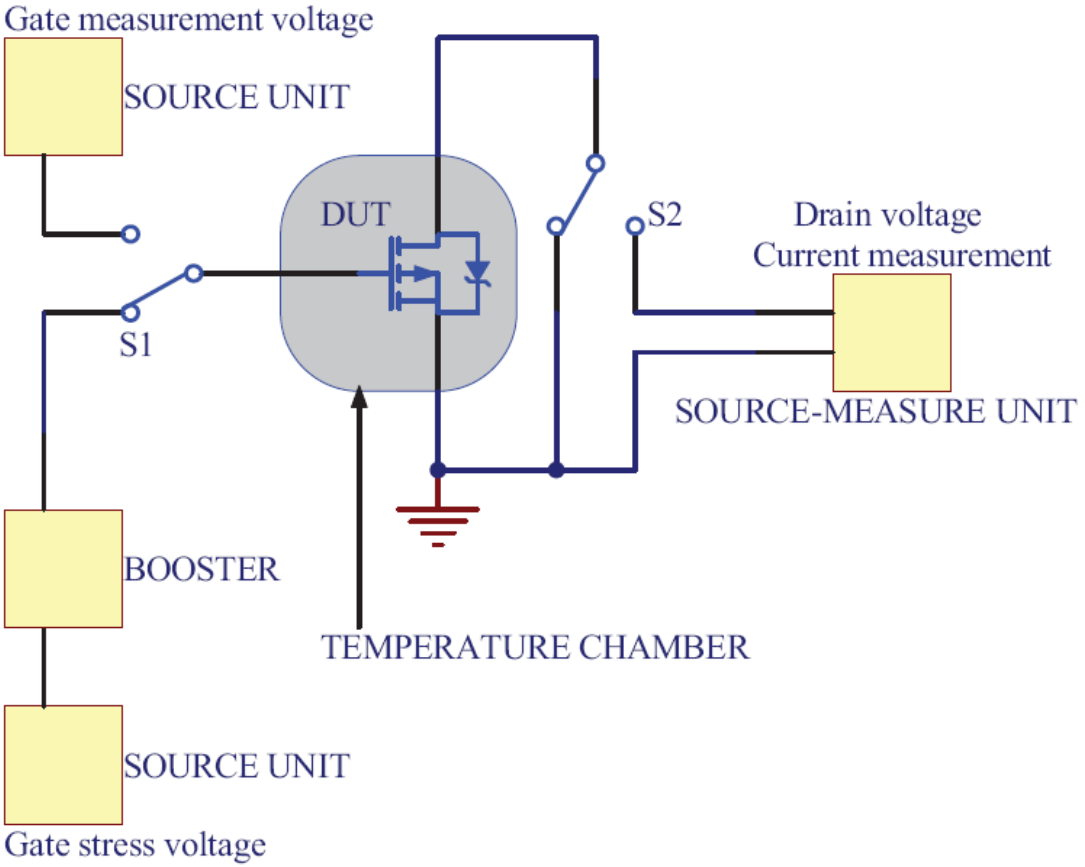
# Experimental details_New Method

- Measurement method: **New Method for NBT Stress and Measuring NBTI Degradation in power VDMOSFETs**



# Experimental details

Block diagram for NBT stress and measurement on p-channel power VDMOS transistor

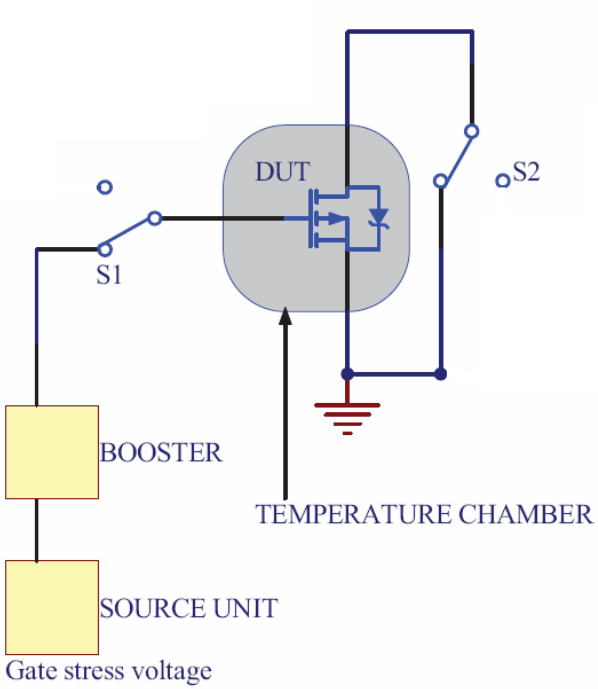



Tektronix AFG3102
Agilent 6645A
Agilent 4156C parameter analyzer
Heraeus HEP2

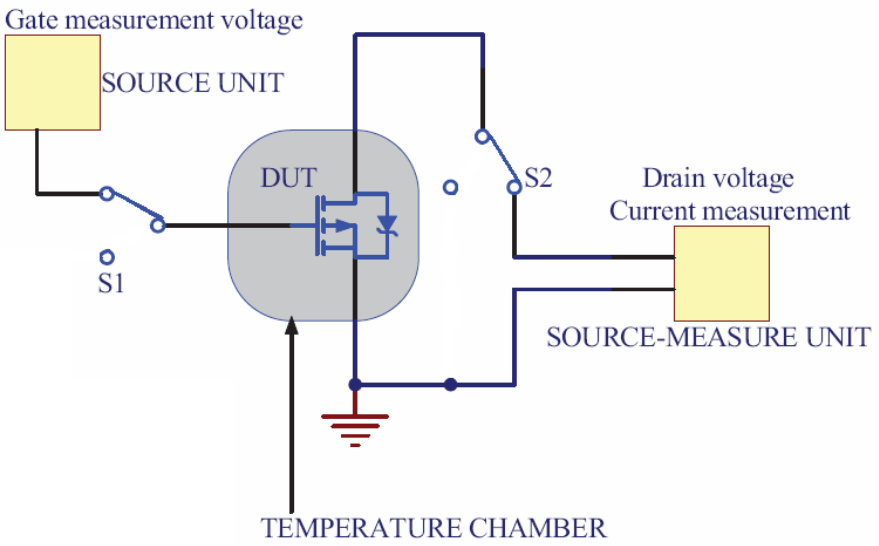
A. Prijić, D. Danković, Lj. Vračar, I. Manić, Z. Prijić, and N. Stojadinović, "A method for negative bias temperature instability (NBTI) measurements on power VDMOS transistors", *Measurement Science and Technology*

# Experimental details

high voltage
stress circuit



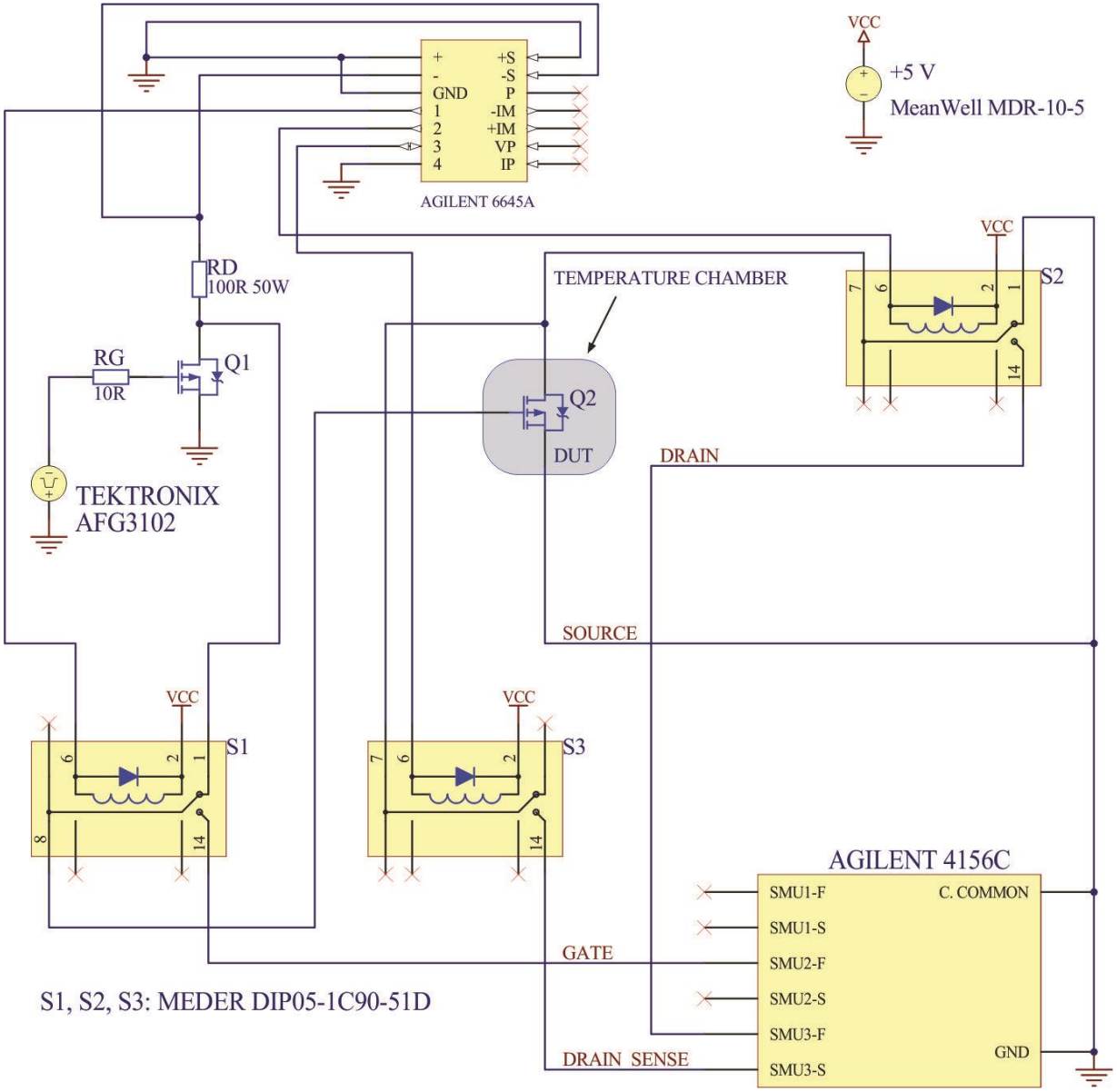

low voltage
measurement circuit




**NBT stress** and **measurement**
on p-channel power VDMOSFETs

# Experimental details

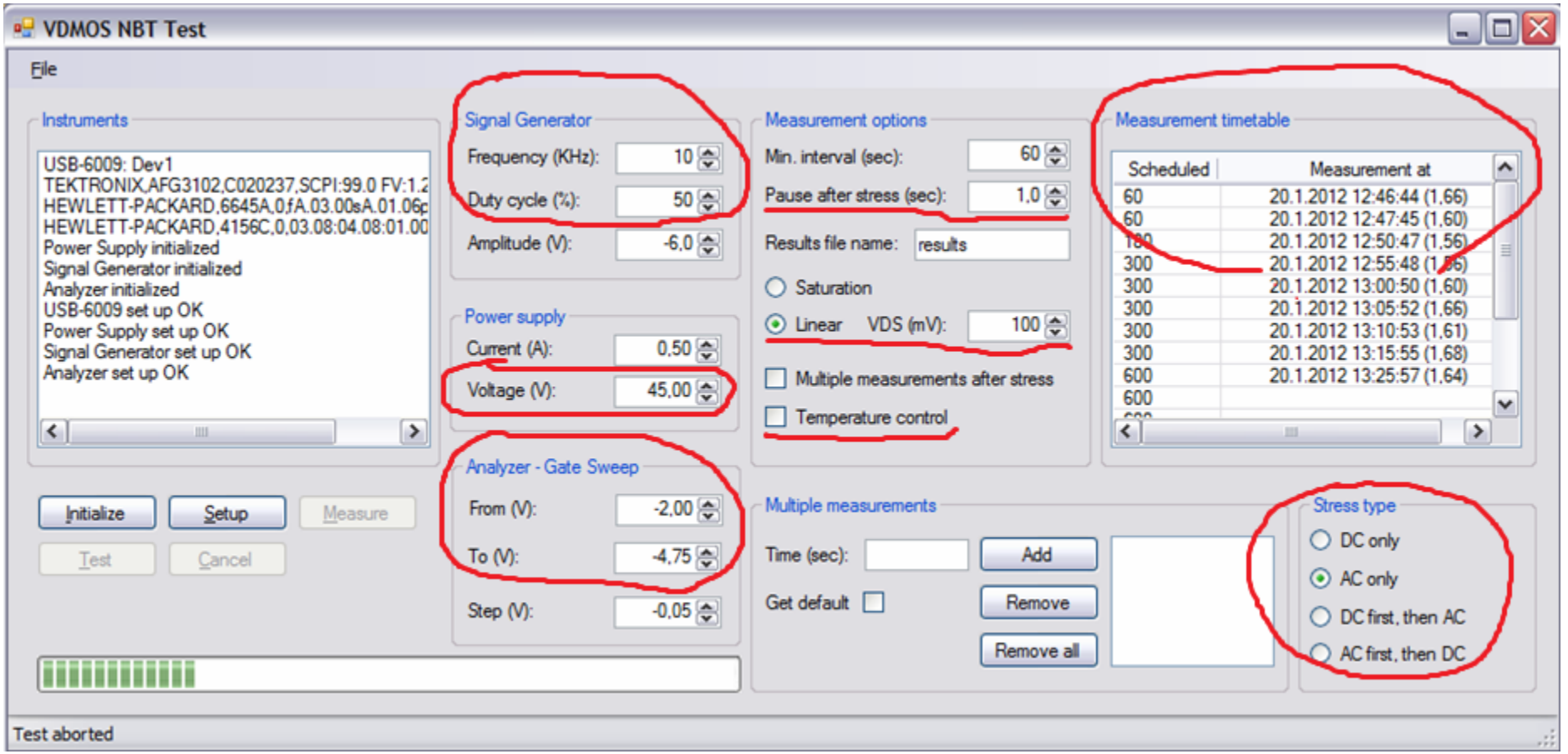
Practical setup for NBT stress and measurement on p-channel power VDMOS transistor




- Tektronix AFG3102
- Agilent 6645A
- Agilent 4156C parameter analyzer
- Heraeus HEP2

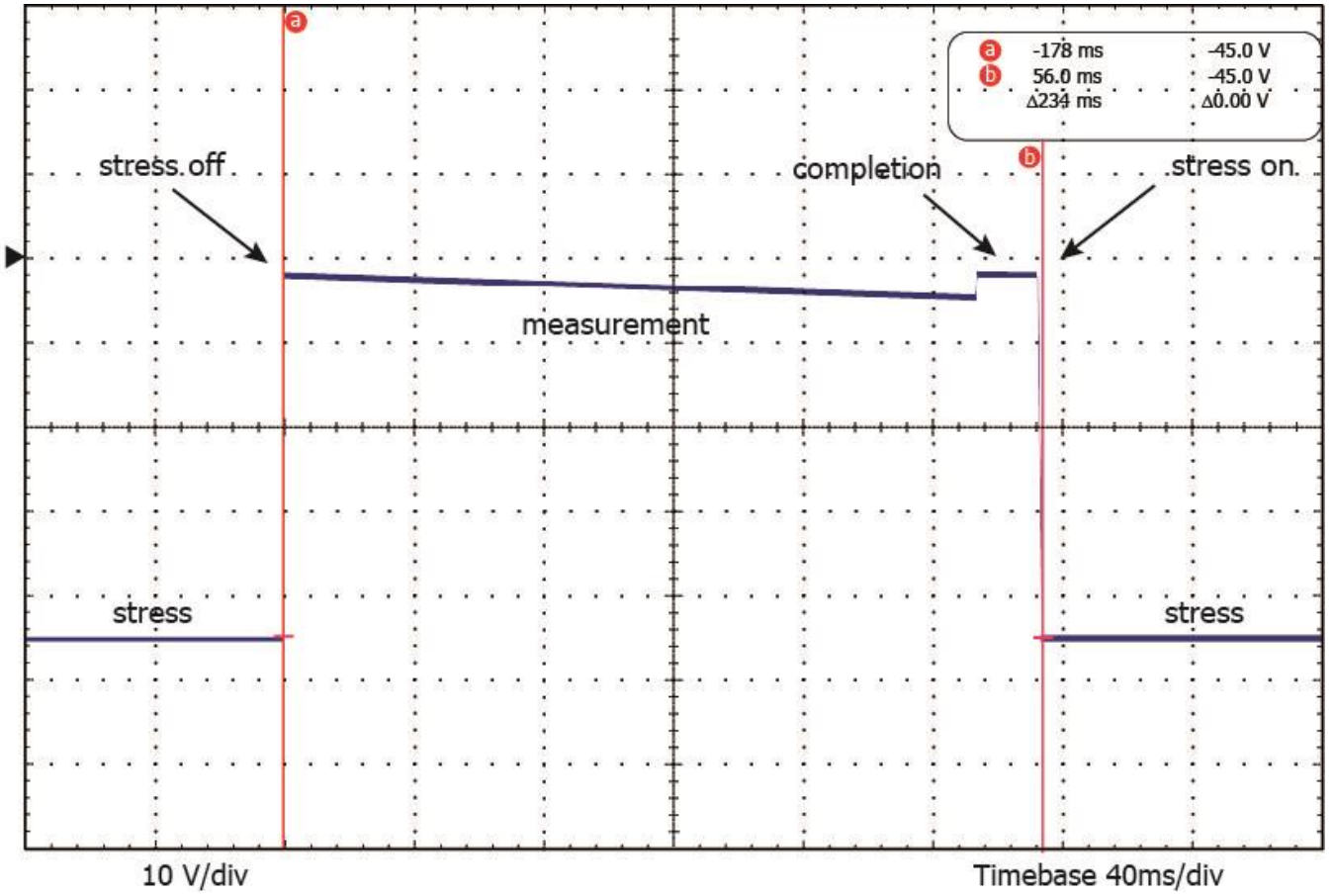
# Graphical user interface

- Computer controlled over IEEE-488 (GPIB) bus.
- PC application software is developed using .NET technology



# The timing sample of the gate voltage

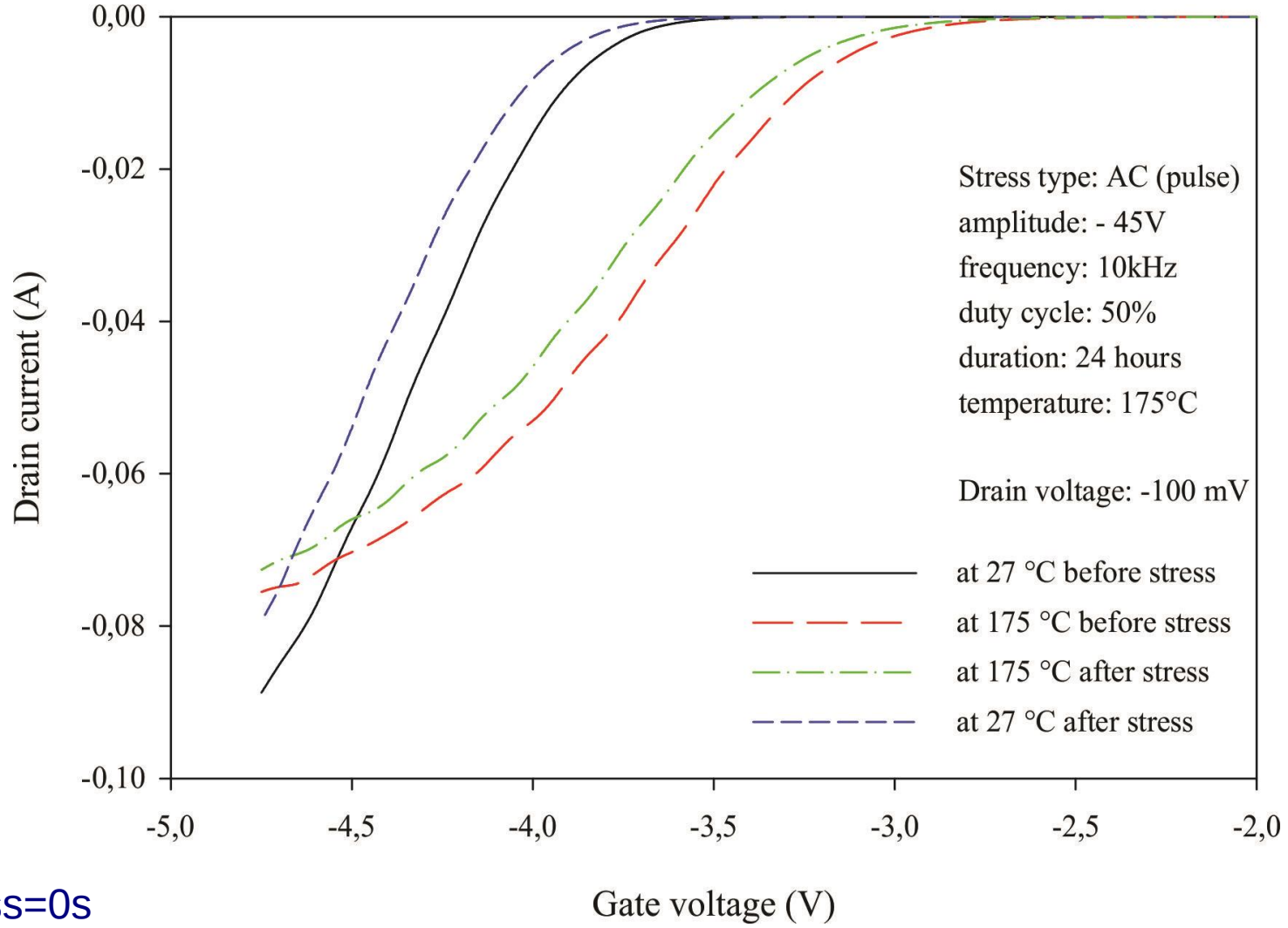
the device remained unstressed for approximately 235 ms !!!




The timing sample of the gate voltage at an interim measurement during the NBTI test (measurement from −2 to −4*.75 V, with* −50 mV step; Tektronix DPO4035 oscilloscope).

# Measurement Setup Verification

Measured transfer *I-V* characteristics




IRF9520

$E_{ox}$ = 4.5MV/cm

$T$ = 175°C

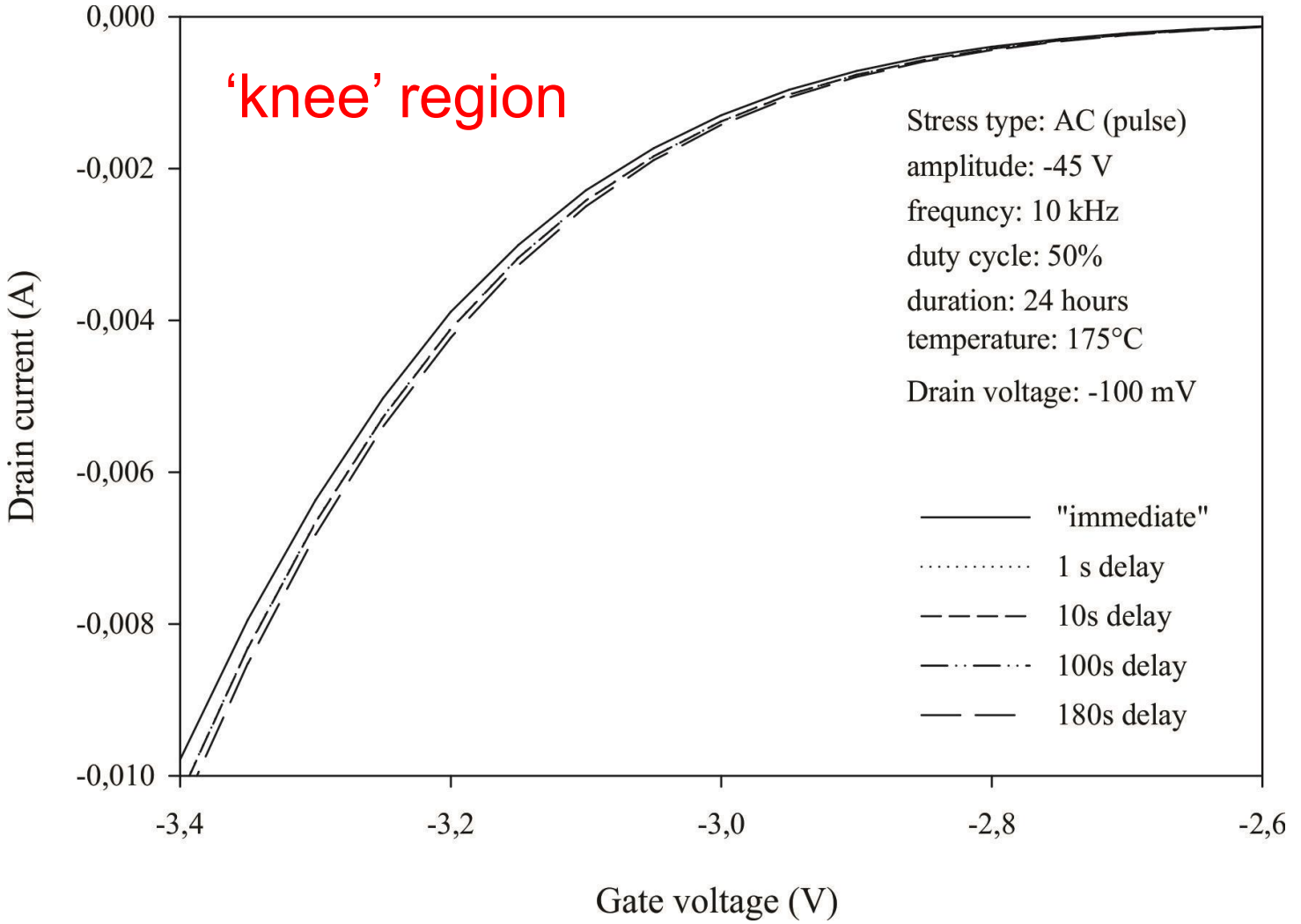
$f$=10kHz

$DTC$=50%

$t_{stress}$ = 24hours

pause after stress=0s

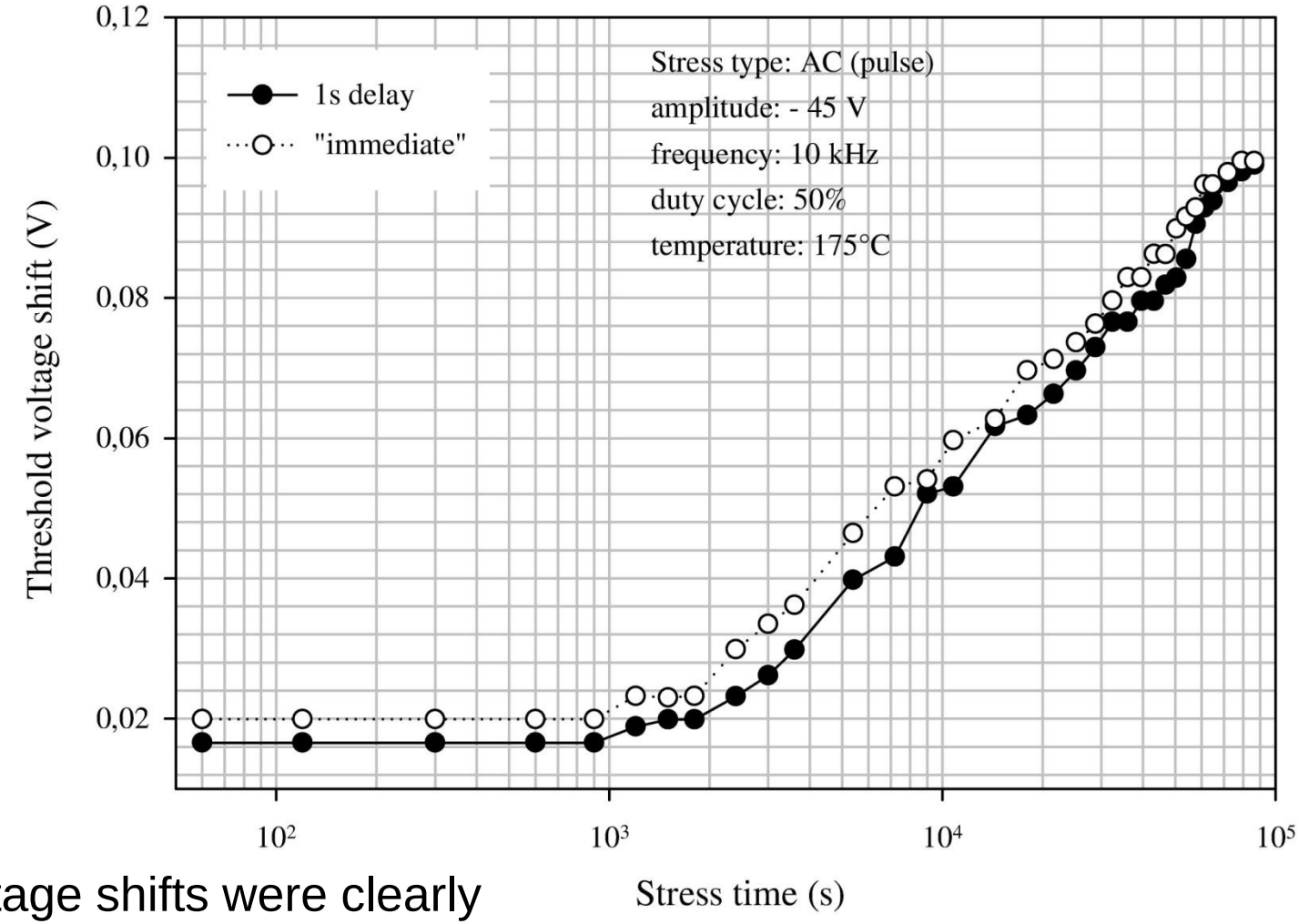
# Measurement Setup Verification




Measured transfer *I-V* characteristics in the ‘knee’ region, illustrating the recovery effect

# Threshold voltage shift

$V_T$ values are calculated from *I-V* characteristics using second derivative method

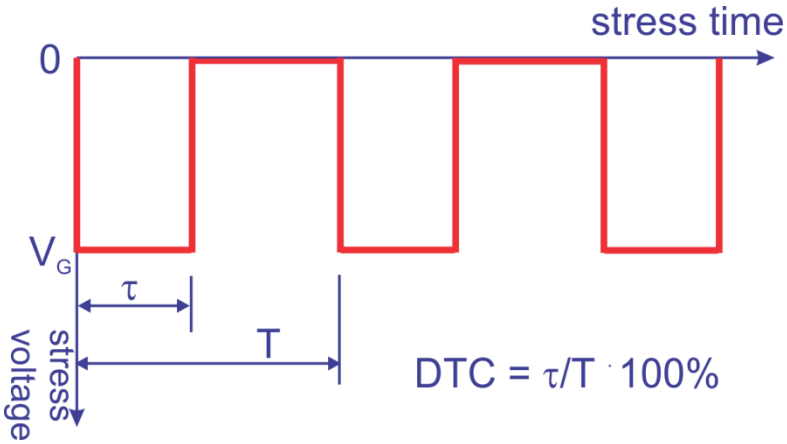



The threshold voltage shifts were clearly more significant when the measurements were performed immediately after the stress

# Experimental results 1st part

## NBT Stressing

| Static | Pulsed |
|---|---|
| up to 36 hours | - |
| negative gate voltage -35, -40, -45 V | - |
| drain and source terminals grounded | - |
| temperature 125, 150,175°C | - |
| | *f*= 10 kHz, *DTC*=50% |



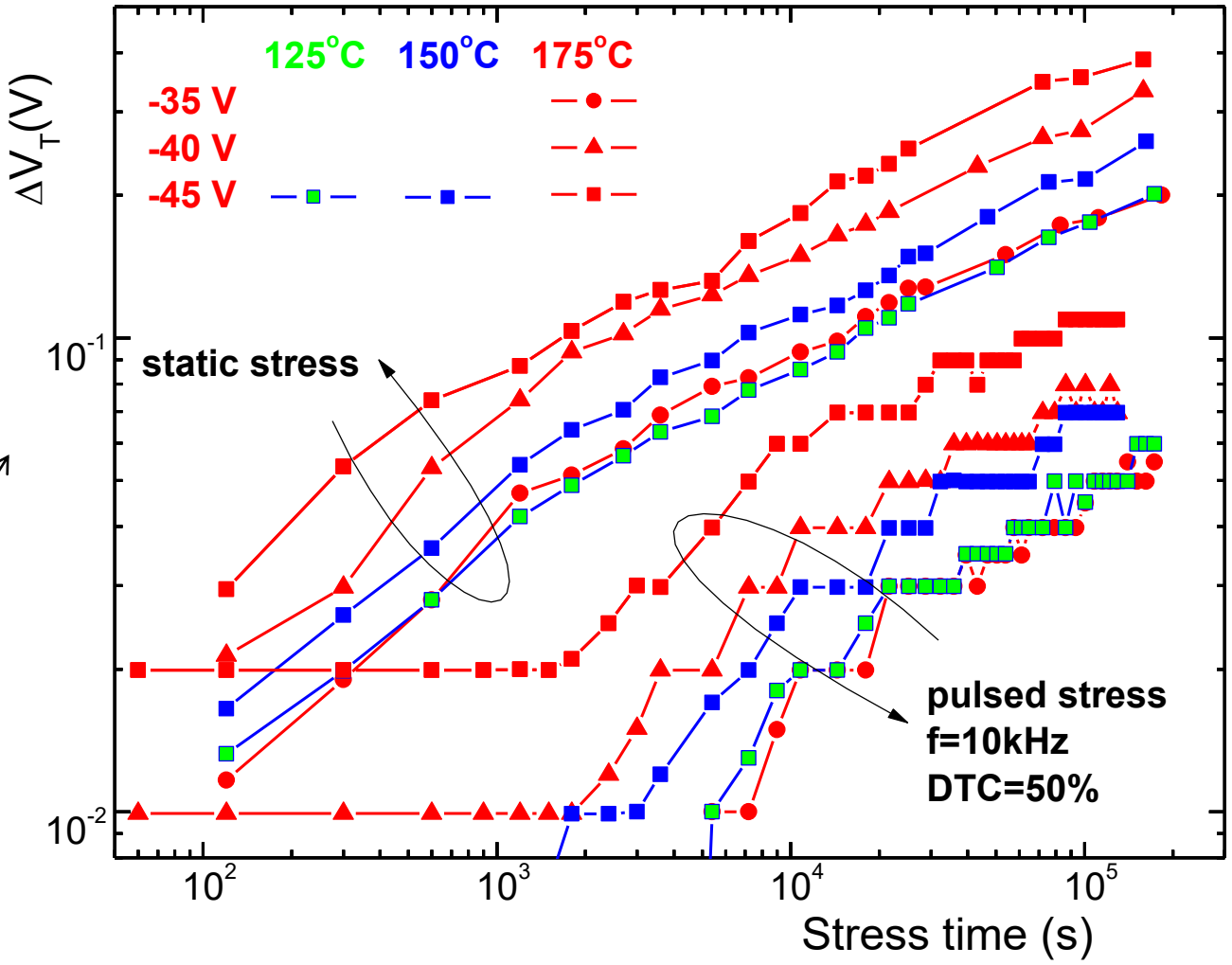

Electrical characterization:

- Transfer I-V characteristics

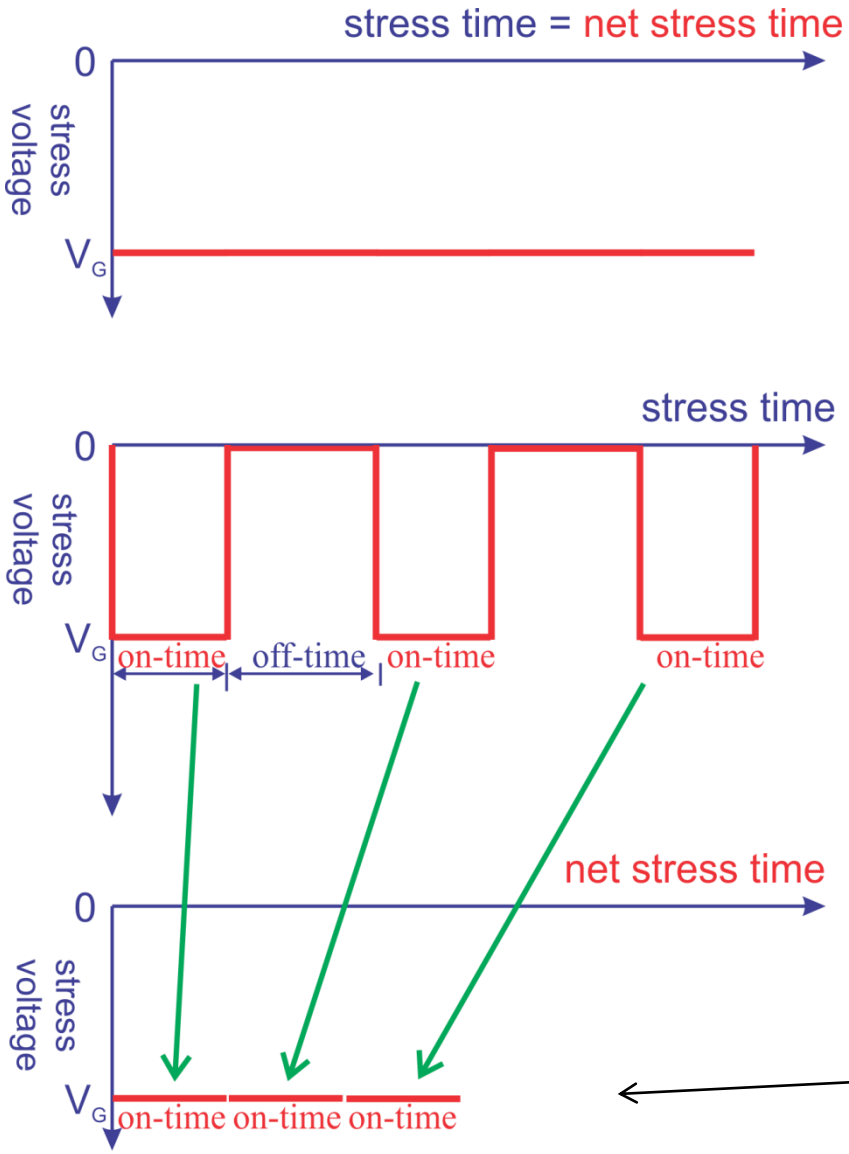
# Threshold voltage shift

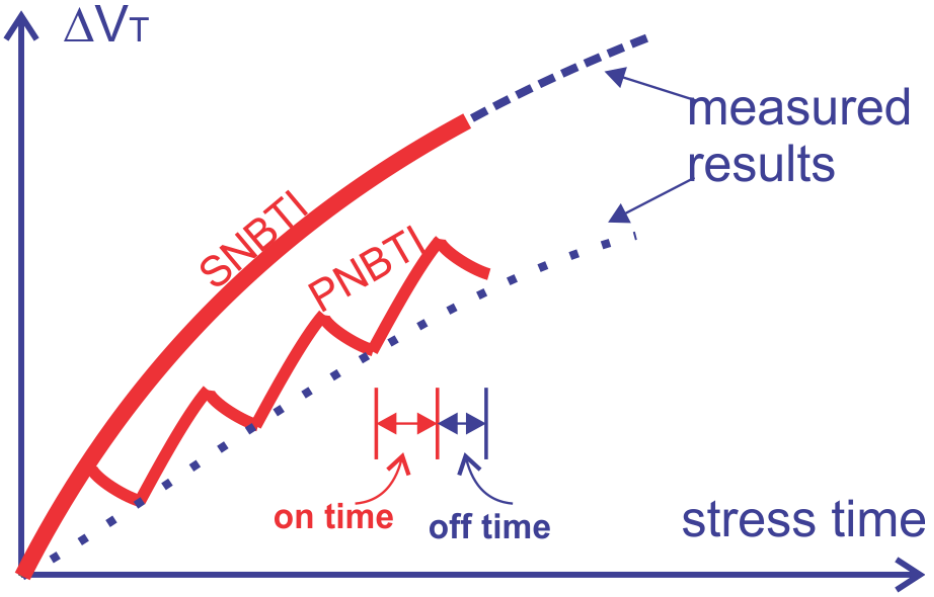
-NBT stressing caused significant $\Delta V_T \nearrow$ $V_G \nearrow$ $T \nearrow$

-$\Delta V_T$ caused by pulsed NBT stress are **lower** than $\Delta V_T$ caused by static NBT stress



# Threshold voltage shift

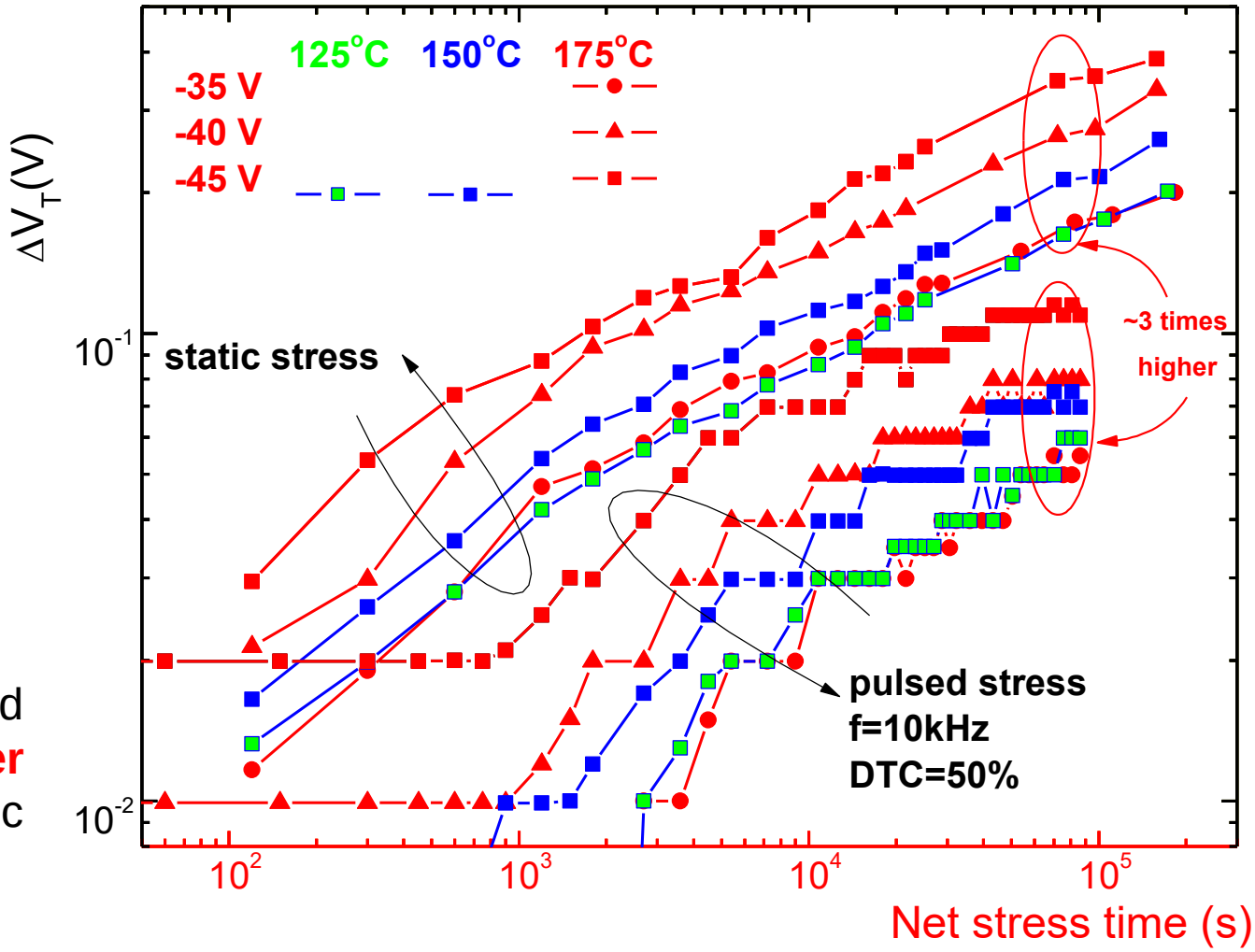



2nd factor- partial (dynamic) recovery

1st factor- different net stress time

# Threshold voltage shift (net stress time)




-$\Delta V_T$ caused by pulsed NBT stress are **still lower** than $\Delta V_T$ caused by static NBT stress

$\Delta V_T$ time dependencies have been affected by partial recovery during off time !!!

# Experimental results 2nd part

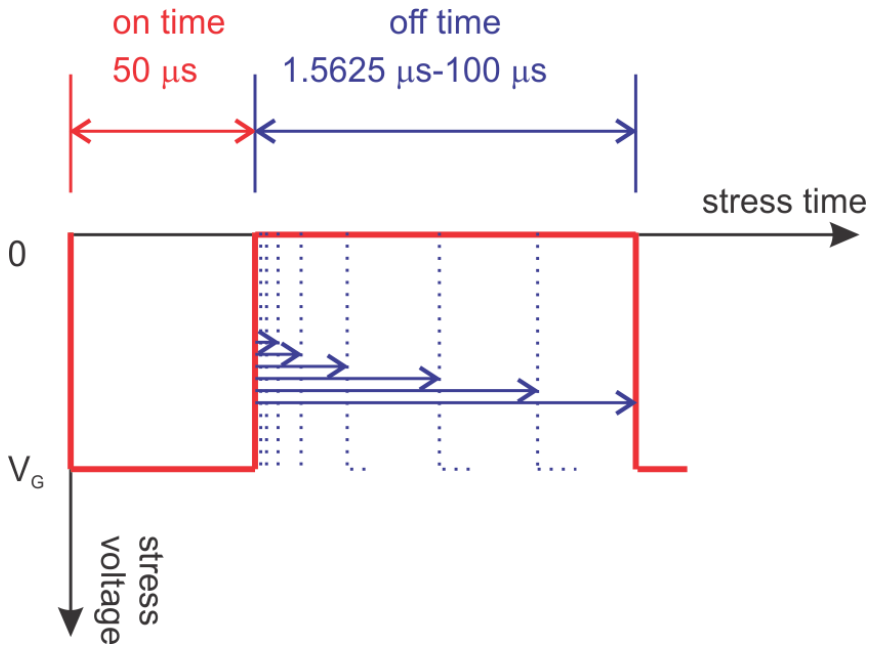
## NBT Stressing

### Pulsed

up to 24 hours
negative gate voltage -45 V
Temperature 175ºC

on time = 50µs = const
off time = varied

T = period = on time + off time
f = 1/period = 1/(on time + off time)
DTC = on time/(on time + off time)
Npulses = 24h/(on time + off time)
Overall net stress time….
Overall recovery time….




### Electrical characterization:

- Transfer I-V characteristics

# Experimental results 2nd part

## on time = 50μs = const, off time = varied

| Stress conditions | Different groups of devices | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Pulse on-time [μs]** | **50** | **50** | **50** | **50** | **50** | **50** | **50** | **50** |
| **Pulse off-time [μs]** | **1.5625** | **3.125** | **6.25** | **12.5** | **25** | **50** | **75** | **100** |
| **Pulse period [μs]** | **51.625** | **53.125** | **56.25** | **62.5** | **75** | **100** | **125** | **150** |
| **DTC [%]** | **96.97** | **94.12** | **88.89** | **80.00** | **66.67** | **50.00** | **40.00** | **33.33** |
| **f [kHz]** | **19.39** | **18.82** | **17.78** | **16.00** | **13.33** | **10.00** | **8.00** | **6.67** |
| **≅Number of pulses for 24h [x$10^9$]** | **1.674** | **1.626** | **1.536** | **1.382** | **1.152** | **0.864** | **0.691** | **0.576** |
| **Net stress time, overall [h]** | **23.27** | **22.59** | **21.33** | **20** | **16** | **12** | **9.6** | **8** |
| **Recovery time, overall [h]** | **0.73** | **1.41** | **2.67** | **4** | **8** | **12** | **14.4** | **16** |

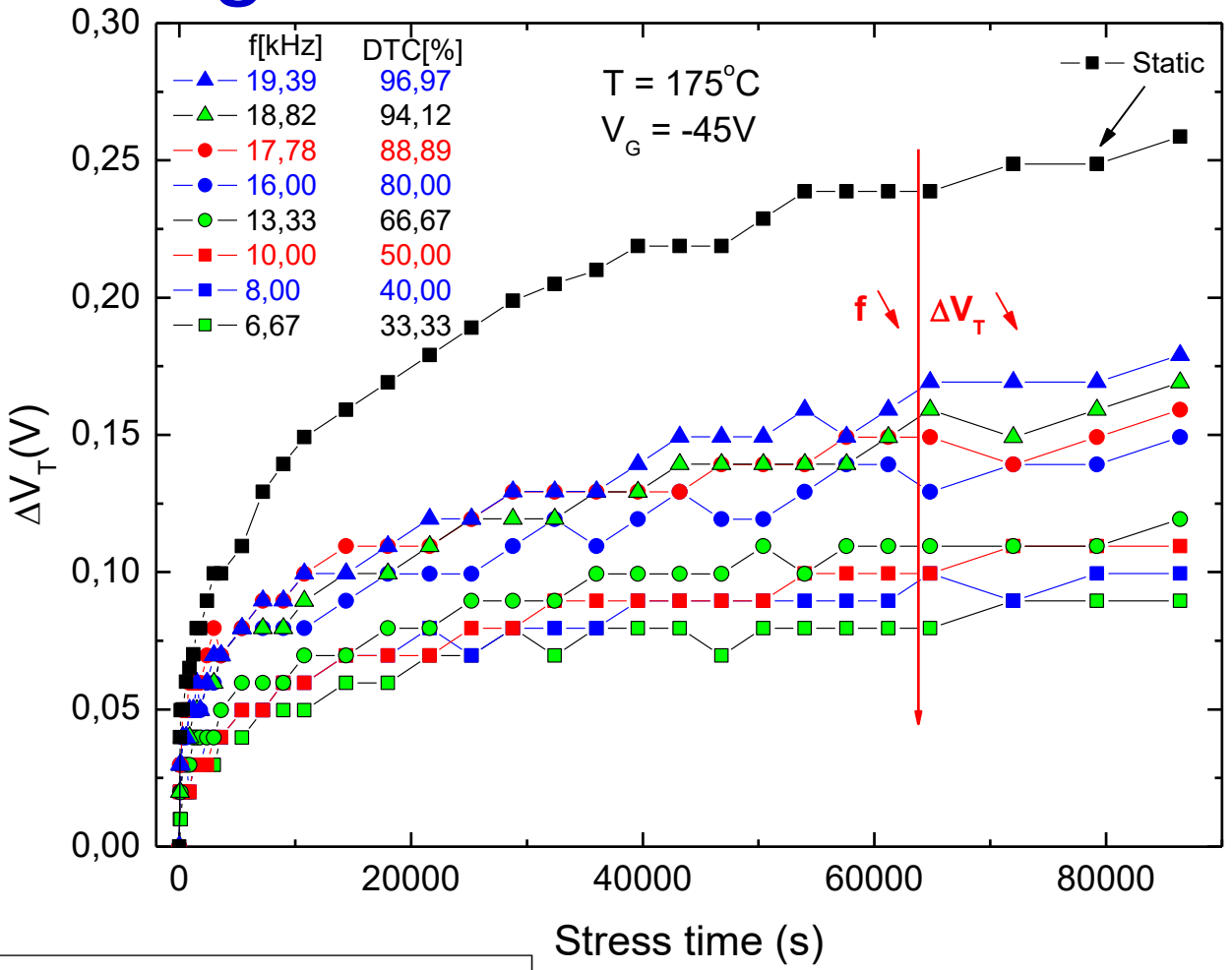
# Threshold voltage shift

NBT stress induced $\Delta V_T$
- most significant for static
- decrease with f ↘ DTC ↘

1st factor:
lower duty cycle (or f)
- same on time
- longer off time

2nd factor:
different number of pulses

lower duty cycle -
fewer pulses and
lesser degradation



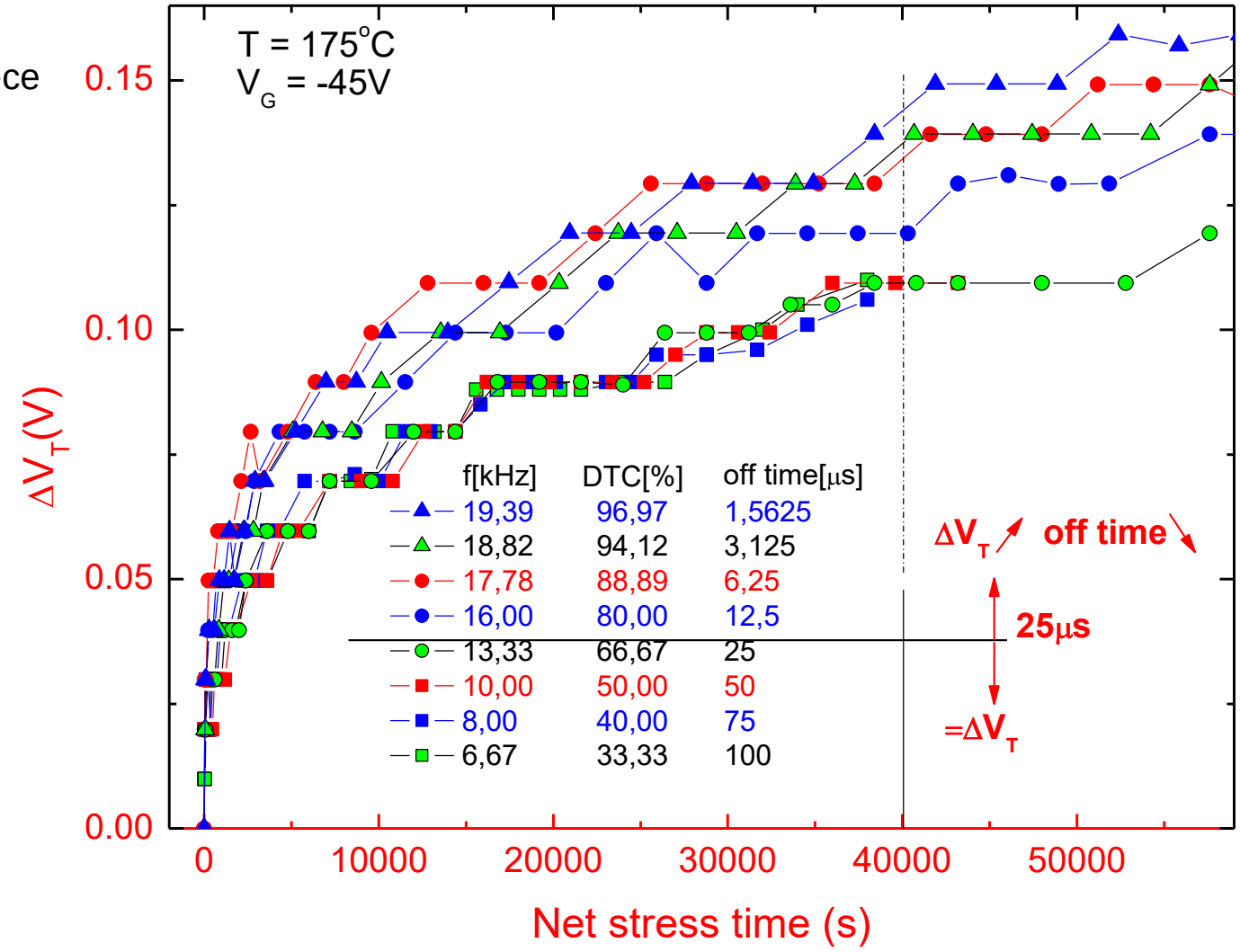

| Stress conditions | Different groups of devices | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Pulse on-time [µs] | 50 | 50 | 50 | 50 | 50 | 50 | 50 | 50 |
| Pulse off-time [µs] | 1.5625 | 3.125 | 6.25 | 12.5 | 25 | 50 | 75 | 100 |
| DTC [%] | 96.97 | 94.12 | 88.89 | 80.00 | 66.67 | 50.00 | 40.00 | 33.33 |
| Number of pulses [x$10^9$] | 1.674 | 1.626 | 1.536 | 1.382 | 1.152 | 0.864 | 0.691 | 0.576 |

# Threshold voltage shift (net stress time)

$\Delta V_T$ vs. net stress time shows complex *f* dependece

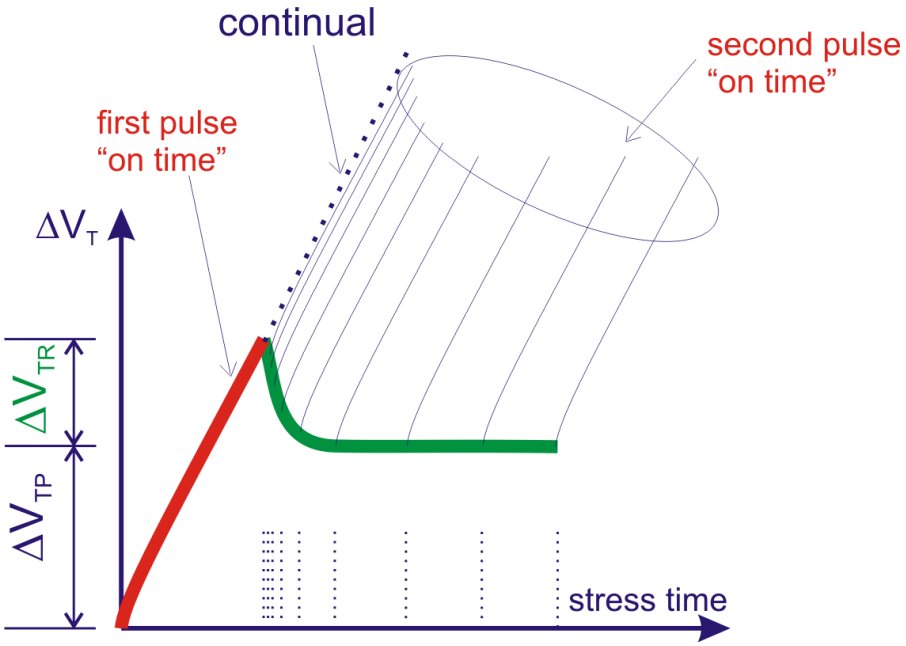
**$\Delta V_T$ are nearly identical**
at f < 13.33kHz
(**off time > 25 μs**)

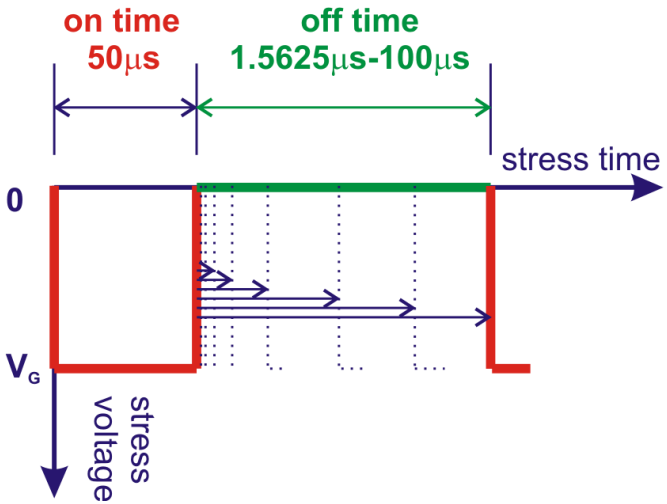
$\Delta V_T$ increasing
f increases
13.33 – 19.39 kHz
(off time 25 -1.5625 μs)




Time constant of 25 μs is very important in the case of pulsed NBT stress !!!

# Threshold voltage shift




- Experimental results have pointed to the existence of characteristic time constant (25 μs) related to the recoverable and permanent components of stress-induced degradation.
- **25 μs off-time** of the pulsed stress voltage was sufficient to **completely remove the recoverable component** of degradation in p-channel power VDMOSFETs.

# Lifetime estimation

# Lifetime estimation

Degradation monitor: stress-induced $\Delta V_T$

Lifetime estimation:

1) Extraction of experimental lifetime values

Experimental lifetime – stress time required for stress-induced $\Delta V_T$ to reach failure criterion (FC) under the given stress conditions ($V_G$, $T$)

FC: $\Delta V_T = 50$ mV

2) Extrapolation to normal operating conditions (gate bias and/or temperature)

# Lifetime estimation – Models

***Voltage models***

$\tau = A \cdot exp(-B \cdot V_G)$ $V_G$ model

$\tau = A_1 \cdot exp(B_1/V_G)$ $1/V_G$ model

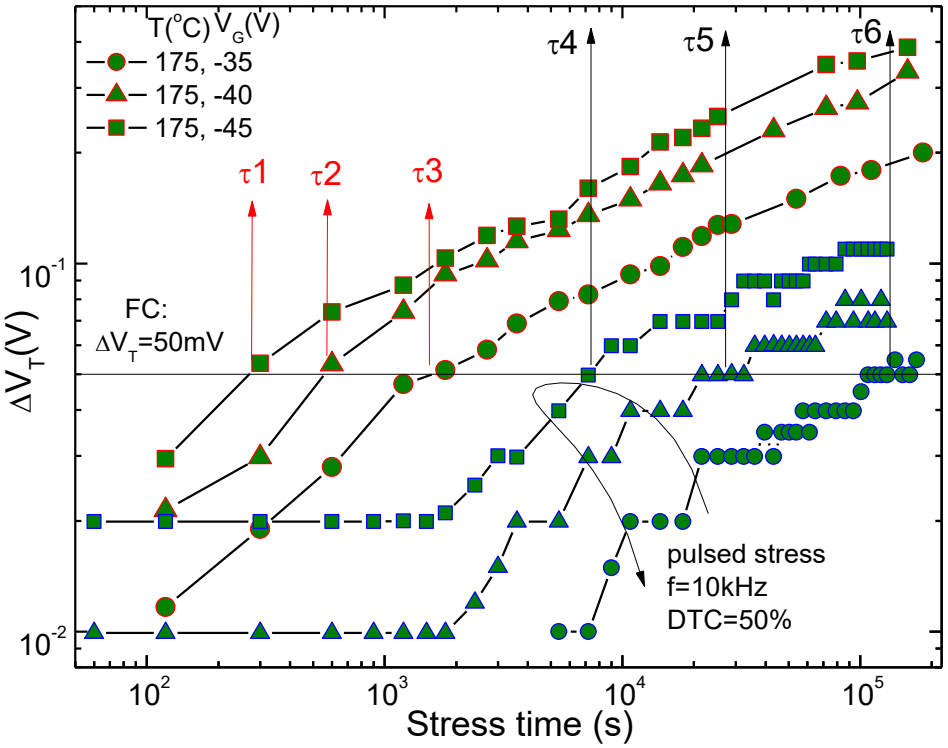
$\tau = C \cdot E\text{-}p$ Power law model

***New temperature model***

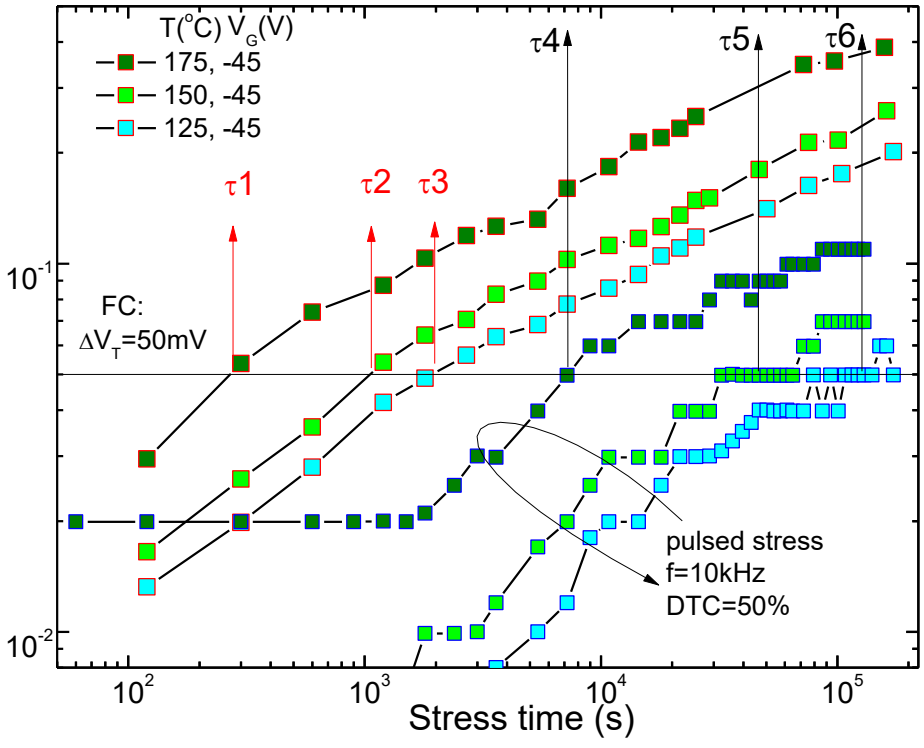
$\Delta V_T = C_1 \cdot Em \cdot tn \cdot exp(-E_d/kT)$

$\tau = A_2 \cdot exp(B_2/T)$

# Extraction of experimental lifetime values




*a*) Extraction using (variable $V_G$, const $T$) data




*b*) Extraction using (const $V_G$, variable $T$) data

Extracted values of experimental lifetime:
- Shorter for higher stress voltages and/or temperatures
- Significantly longer in the case of pulsed NBT stressing

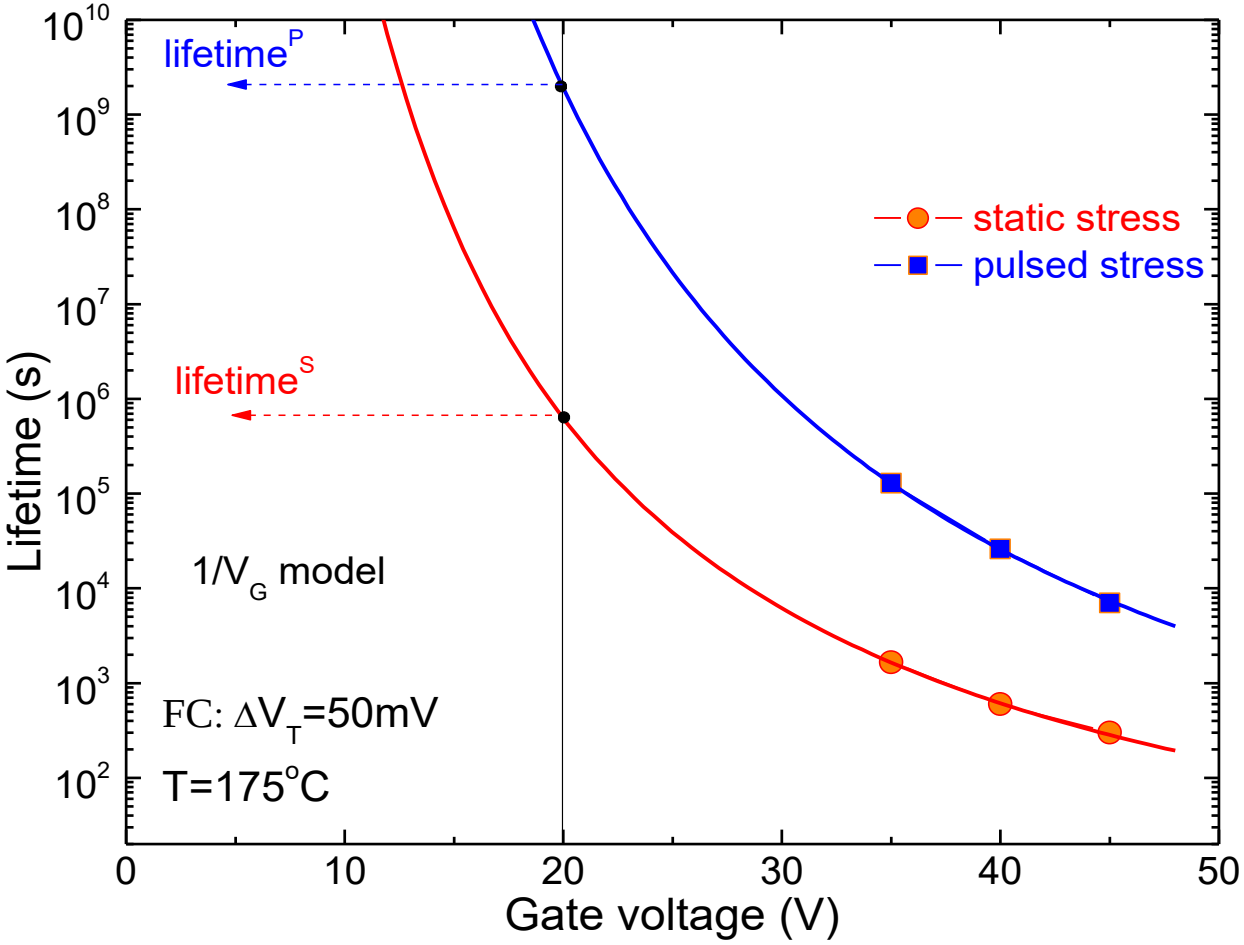
# Extrapolation to normal operating conditions

Extrapolation along the **voltage axis**:

◊ exp. $\tau$ values extracted from (variable $V_G$, const $T$) data – (*a*)

◊ extrapolation model derived from a degradation model for stress-induced $\Delta V_T$ (power law, $V_G$, or $1/V_G$ model)

**$1/V_G$ model**




Extrapolation to:

- $V_G$ = 20 V → $\tau$ (lifetime) over three orders of magnitude higher under the pulsed gate bias conditions

Devices may maintain proper functionality for much longer period under the pulsed gate bias conditions than if kept constantly under the dc bias

Extrapolation can be done to any gate voltage, but only for the temperature used in the NBT stress experiment

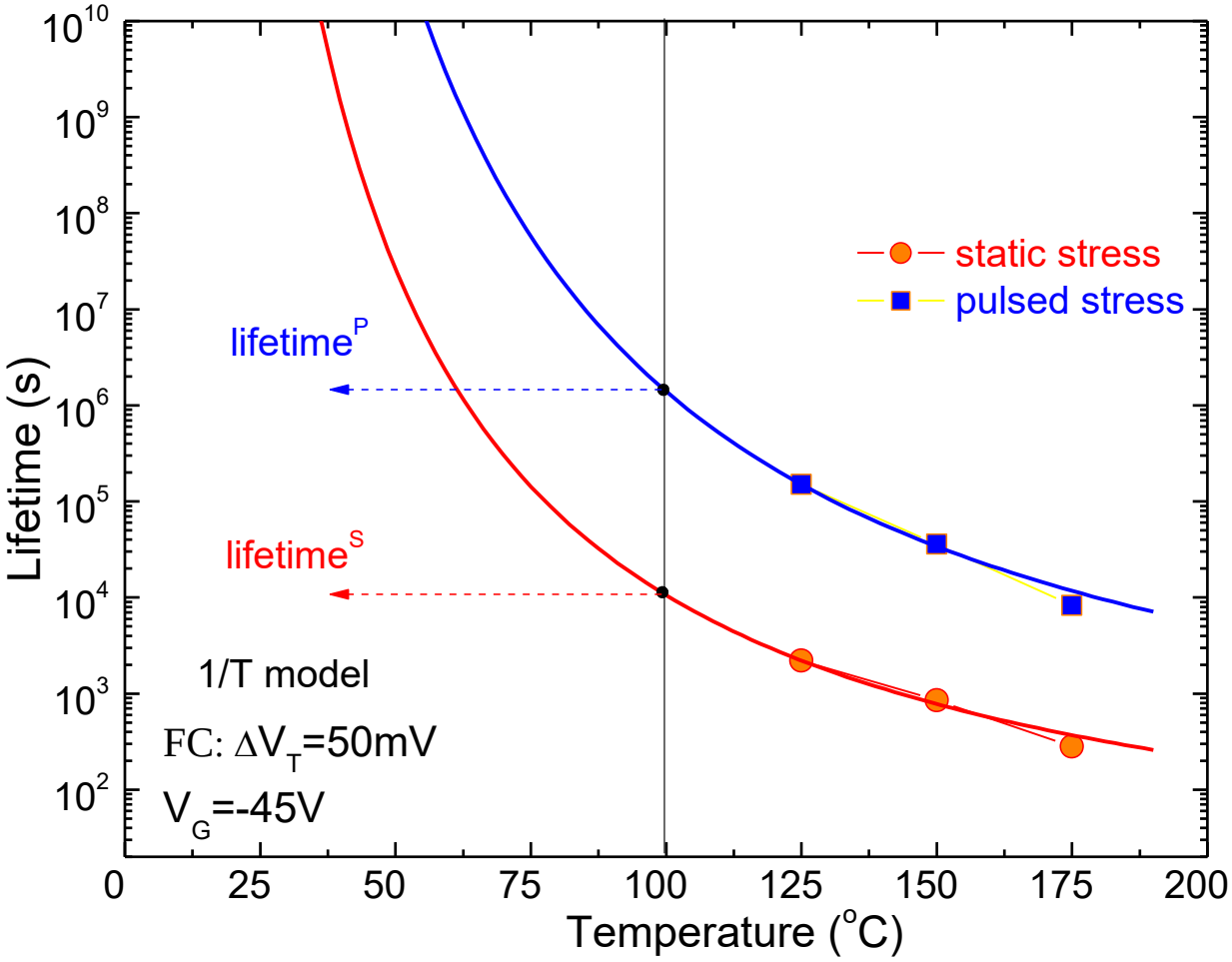
# Extrapolation to normal operating conditions

Extrapolation along the **temperature axis** :

◊ exp. $\tau$ values extracted from (const $V_G$, variable $T$) data – (*b*)

◊ extrapolation model derived from a degradation model for stress-induced $\Delta V_T$

**"1/*T* model"**




Extrapolation to:

- $T$ = 100 ℃ → $\tau$ (lifetime) over two orders of magnitude higher under the pulsed gate bias conditions

Devices may maintain proper functionality for much longer period under the pulsed gate bias conditions than if kept constantly under the dc bias

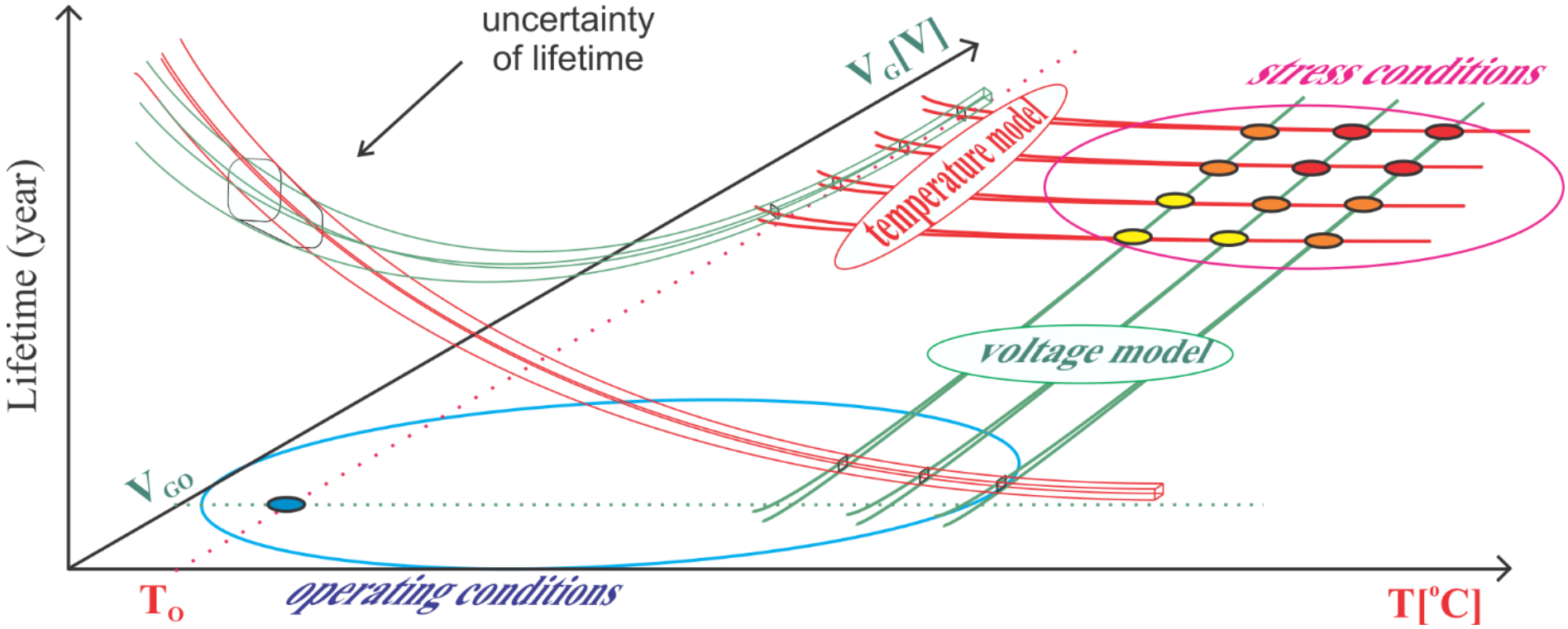
Extrapolation can be done to any temperature, but only for the gate voltage used in the NBT stress experiment

# Double extrapolation along both voltage and temperature axes

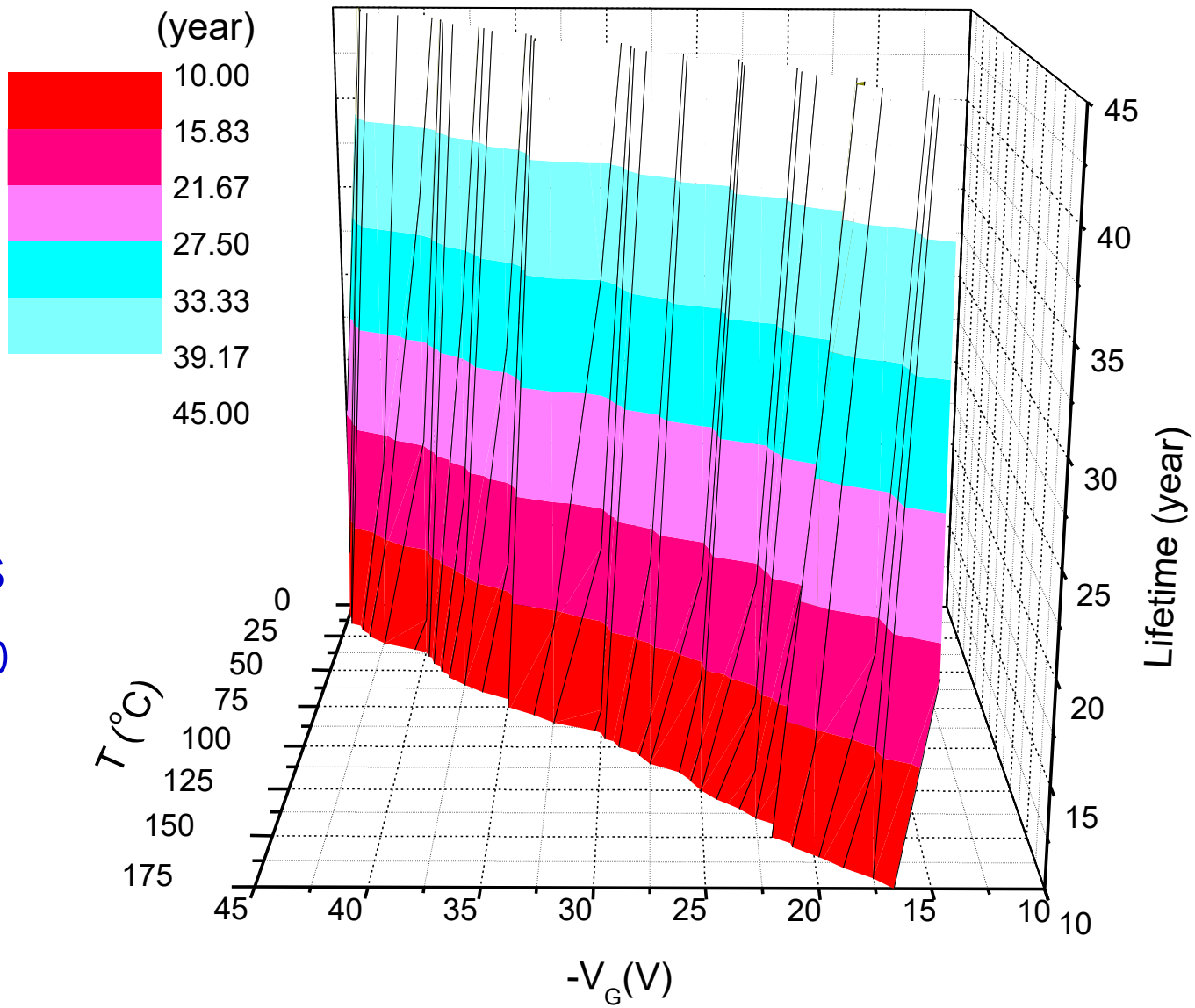
| Stress | -35 V | -40 V | -45 V | | -20 V |
|---|---|---|---|---|---|
| 125 ℃ | o | o | o | → **1/$V_G$** → | **o** |
| 150 ℃ | o | o | o | → **1/$V_G$** → | **o** |
| 175 ℃ | o | o | o | → **1/$V_G$** → | **o** |
| | ↓ | ↓ | ↓ | | ↓ |
| | **1/T** | **1/T** | **1/T** | | **1/T** |
| | ↓ | ↓ | ↓ | | ↓ |
| **100 ℃** | **o** | **o** | **o** | → **1/$V_G$** → | **o** |

Legend:
o – experimental lifetime data
**o** – lifetime data obtained by 1/$V_G$ model
o – lifetime data obtained by 1/T model
o – lifetime obtained by double extrapolation

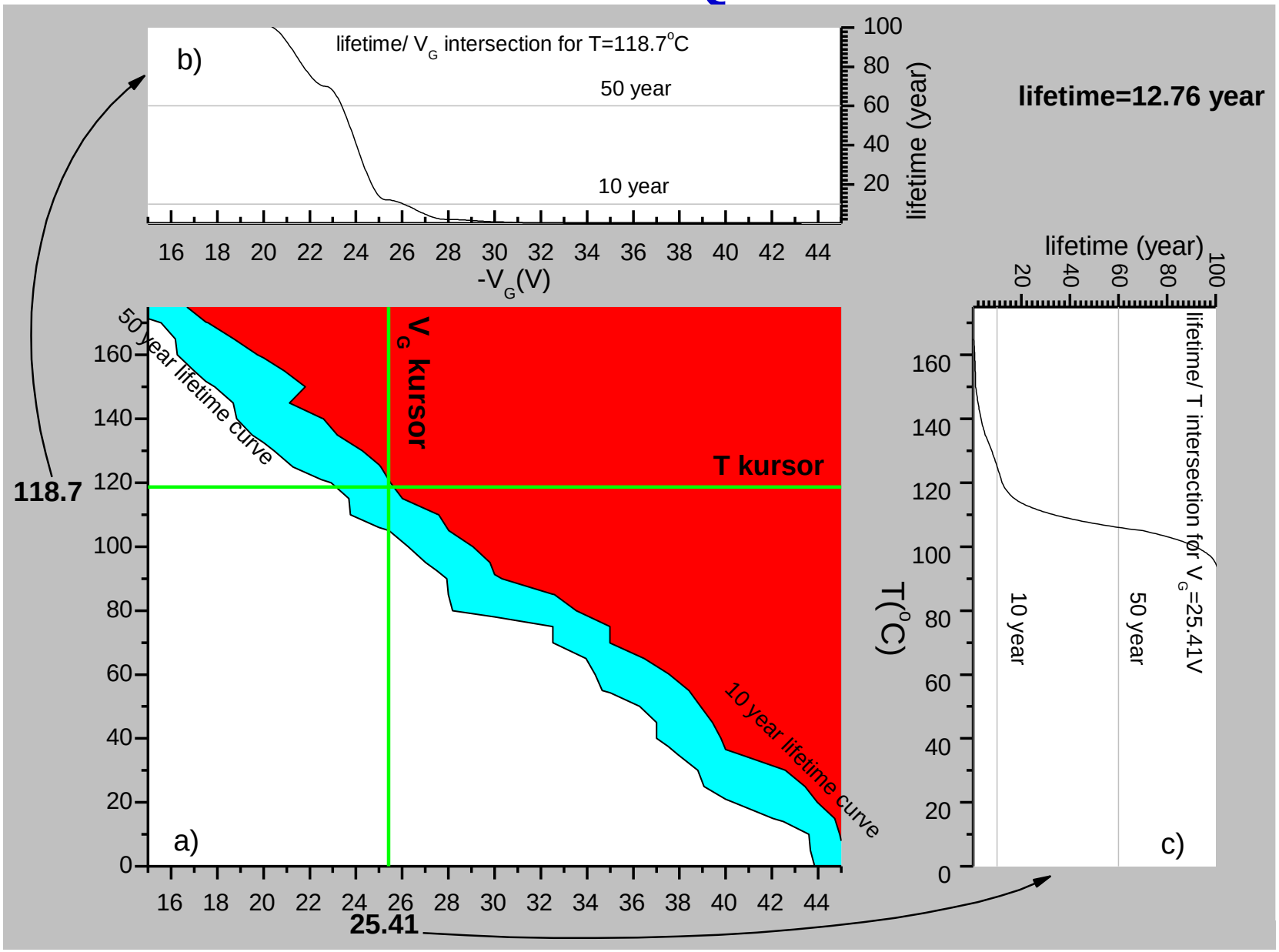
# Double extrapolation
## along both voltage and temperature axes



# Lifetime estimation – 3D surface area



# Lifetime estimation – Quasi 3D simulator



# NBTI & IRRADIATION

# Experimental results 3rd part

In some applications p-channel VDMOSFETs may be the subject of simultaneous irradiation and NBT stressing

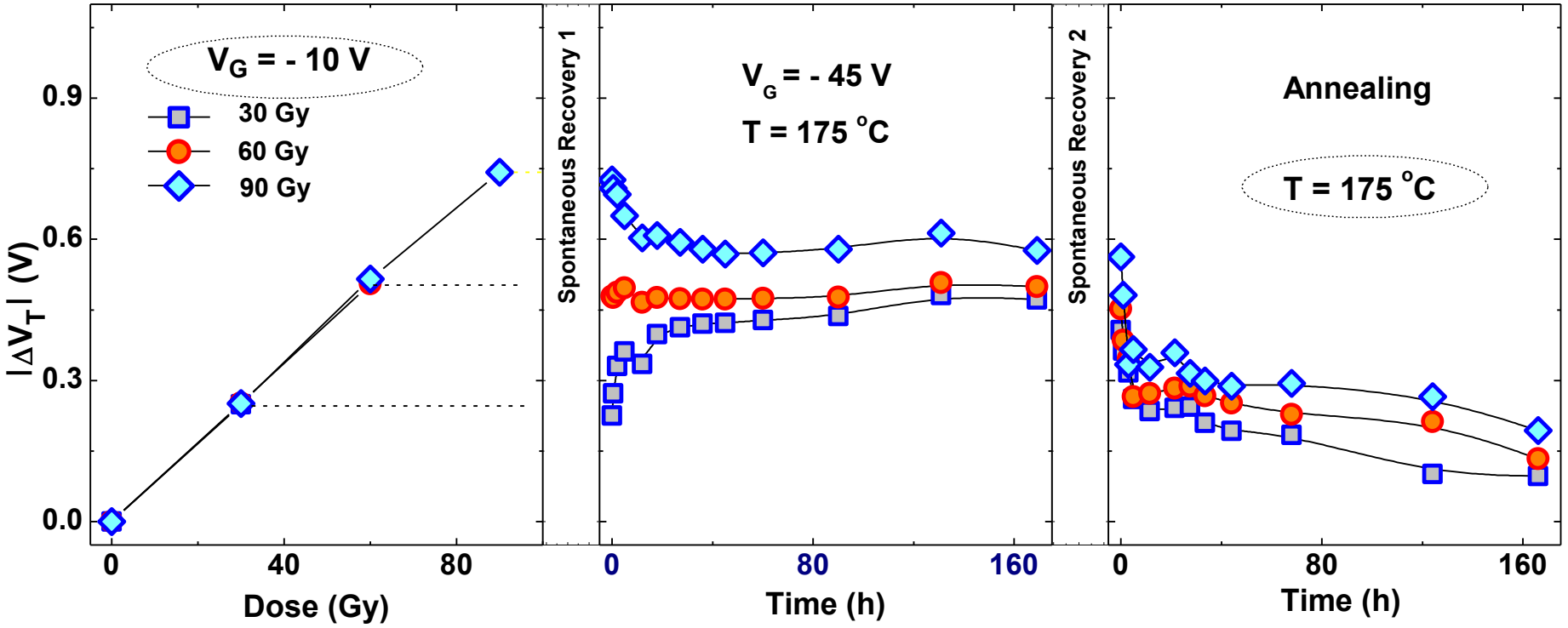
| **IRRADIATION** | **NBTS** | **Annealing** |
|---|---|---|
| | Static | |
| dose 30 Gy, 60 Gy, 90 Gy | 168 hours | 168 hours |
| negative gate voltage -10 V | -45 V | 0 V |
| temperature, room | 175°C | 175°C |

drain and source terminals grounded

Electrical characterization:

- Transfer I-V characteristics

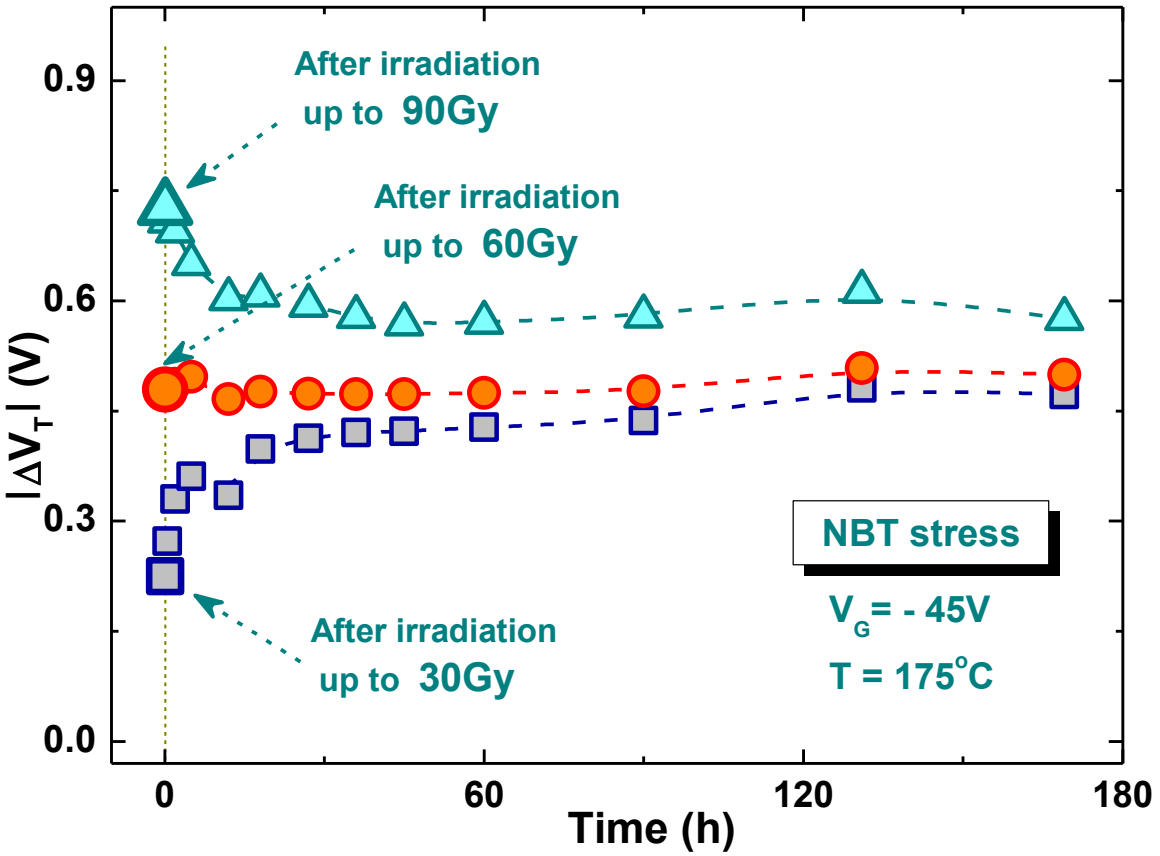
# RAD&NBTS – Time dependencies of $\Delta V_T$




NBT stress of irradiated devices caused
different threshold voltage behaviour strongly dependent on total dose received:

-in the case of highest total dose (90 Gy) it has actually lead to the decrease of $V_T$ shift,
-for total dose of 60 Gy threshold voltage shift was almost negligible,
-in the case of lowest total dose (30 Gy) subsequent NBT stress induced further negative $V_T$ shift.

# NBTS – Time dependencies of $\Delta V_T$




It is obvious that two mechanisms might be responsible for the effects observed during the post-irradiation NBT stress:

(i) activation of electrochemical reactions contributing to NBTI, which leads to additional creation of Not and Nit,

and

(ii) annealing of irradiation-induced oxide charge and interface traps due to high temperature (175°C) applied.

# Conclusions

- A description of a method suitable for NBTI measurements on p-channel VDMOS transistors was presented.
- Stress-induced degradation under the pulsed stress conditions was shown to be generally lower than in the case of static NBT stress.
- 25 μs off-time of the pulsed stress voltage was sufficient to completely remove the recoverable component of degradation.
- The use of voltage and temperature models for extrapolation to normal operation voltage and temperature is demonstrated.
- New approach in estimating the device lifetime, which assumes double extrapolation along both $V_G$ and $T$ axes, was proposed.
- Quasi 3D simulator for lifetime estimation in all kinds of MOS transistors, independent on production technology, was developed.
- Results of sequentially irradiation and NBT stressing were presented.